JPL Publication 92-22

Field Programmable Gate Arrays: Evaluation Report for Space-Flight Application

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September 15, 1992

National Aeronautics and
Space Administration

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The research described in this publication was carried out by the Jet Propulsion Laboratory (California Institute of Technology), Aerospace Corporation, Actel Corporation, Applied Physics Laboratory, GE Astro Space, Hughes Aircraft, TRW, Magnavox Electronics Systems Company, and the National Aeronautics and Space Administration.

SPECIAL ACKNOWLEDGEMENT

The content of this report was provided by the following organizations:

JET PROPULSION LABORATORY

AEROSPACE CORPORATION

ACTEL CORPORATION

APPLIED PHYSICS LABORATORY

GE ASTRO SPACE

HUGHES AIRCRAFT

TRW

MAGNAVOX ELECTRONICS SYSTEMS COMPANY

This publication was prepared by the Jet Propulsion Laboratory, California Institute of Technology under agreement with the aforesaid consortium members and others whose work contributed to the overall FPGA evaluation. It is distributed for information purposes only.

ABSTRACT

Field Programmable Gate Arrays commonly called FPGA's are the newer generation of field programmable devices and offer more flexibility in the logic modules they incorporate and in how they are interconnected. The flexibility, the number of logic building blocks available, and the high gate densities achievable are why users find FPGA's attractive. These attributes are important in reducing product development costs and shortening the development cycle. The aerospace community is interested in incorporating this new generation of field programmable technology in space applications. To this end a consortium was formed to evaluate the quality, reliability, and radiation performance of FPGA's. This report presents the test results on FPGA parts provided by ACTEL Corporation.

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ACRONYMS

AC	alternating current
ASIC	Application Specific Integrated Circuit
BPSG	borophosphosilicate glass
DPA	destructive physical analysis
FPGA	Field Programmable Gate Array
I/O	input/output
IOL	current output low
LET	linear energy transfer
mA	milliamps
MeV	million electron volts
PIE	post-irradiation effects
PIP	Parts Information Program
SEE	single event effects
SEM	scanning electron microscope
SEU	single event upset
TID	total ionizing dose
TPHL	transition propagation delay high to low
TPLH	transition propagation delay low to high

SECTION 1.0
GENERAL

1.1 BACKGROUND

ACTEL Corporation's Field Programmable Gate Arrays (FPGA's) have been of interest to the aerospace community for the last two years. The Electronics Parts Reliability Section of the Jet Propulsion Laboratory started evaluating the ACT I A1010/A1020 (2-μm process) product family only to discover that this series was to be discontinued. The new enhanced ACT II A1280 (1.2-μm process) family was to be the replacement and would provide higher density and an attractive option to both JPL and the aerospace community. The early evaluations begun on the ACT I continued to the ACT II family through a consortium that was formed between JPL, Aerospace Corporation, TRW, and Hughes Space and Communication Division. This consortium was a means to expedite the ACT II evaluation. Aerospace Corporation volunteered to perform SEU testing, TRW would do transient dose rate, Hughes Space Division would do TID, and JPL would do construction analysis, electrical characterization, life test, coordinate the activities, and write the final report. ACTEL provided military temperature screened, unprogrammed parts to the various consortium members for their evaluations. Besides the original consortium members, other interested parties such as Applied Physics Laboratory (APL), Magnavox Electronic Systems, and GE Astro Space were conducting radiation tolerance evaluations. Their findings are also included in this report.

The information and knowledge obtained are the culmination of effort and successful collaboration of the consortium and others. The test results and performance data retrieved demonstrate the value of a consortium sharing information and thus reducing costs and schedules for all.

1.2 INTRODUCTION

ACTEL-designed Field Programmable Gate Arrays (FPGA's) manufactured by Matsushita Electronics Corporation have been evaluated for their suitability in space applications. The FPGA's are manufactured on a commercial manufacturing process as opposed to a radiation-hardened manufacturing process. A number of design and cost tradeoffs make the commercial FPGA an attractive alternative to other ASIC technologies. The short design cycle and relatively low cost are an immediate advantage. ACTEL's proven oxide-nitride-oxide antifuse reliability also warranted looking at these FPGA's for space applications.

The areas of special interest and evaluation conducted by JPL and others included metalization integrity, radiation tolerance from total dose damage, single event effects sensitivity,

and device latchup caused from heavy ions. In addition a number of parts were put on life test. They were examined using destructive physical analysis methods before and after 2000 hr of life. From some of the data and analysis some lifetime predictions were made within the constraint of design rules and particular application. Because the ACTEL FPGA is not manufactured on a radiation-hardened process, it is important to review the results in light of the inherent capabilities of the device and design with the current process technology. With this in mind, some standard benchmark can be established to give the user some guidance for performance. The results reported do not always agree because test methods and device configurations were not identical. However, based on the data obtained and assimilated an expected level of behavior can be predicted for the FPGA devices. It is up to the user to do further testing if needed to satisfy a more stringent requirement. This report and its findings in general support the ACTEL FPGA technology for some space applications and conditions.

The report is divided into four sections. The first section is the general section comprising the general comments and conclusions by JPL. The remaining sections are a summary of the work and supporting data for the A1020 (2-μm), A1280 (1.2-μm), and A1020A (1.2-μm) FPGA's. The sources and authors for these summaries are referenced. The work was done independently yet together completes the objective to evaluate the FPGA technology. The technical content of the charts and graphs is presented exactly as taken from the sources. Interpretation is left to the reader because the data were from limited sample sizes, which may not be statistically valid.

1.3 DESTRUCTIVE PHYSICAL ANALYSIS EVALUATION

The work done by JPL focused on destructive physical analysis for the A1020 (2.0 μm) and 1280 (1.2 μm). Devices from these two FPGA technologies were examined in detail by cross-section analysis of all materials and their respective thickness and interface pattern. The DPA reports for the ACT I A1020 and ACT II A1280 are included as JPL PIP report Nos. 304 and 305. In general the die structures and measurements made from SEM photographs were in agreement with information provided by ACTEL.

The only concern is the evidence of metal-2 thinning in a via step to metal-1 and in metal step coverage in BPSG cuts to poly and silicon contacts. The measured thickness was 25% or less of nominal metal thickness. This violates MIL-STD-883 Method 2018.3 paragraph 3.7.2. This limited metal step coverage was seen in both the 2.0-μm and 1.2-μm technology and corroborated by evaluation at TRW. The 1.2-μm technology is more aggravated because of the scaling effects of metal and subsequent smaller via and contact sizes.

In order to ascertain the reliability risk created by the step coverage, current density calculations were done for single contacts. MIL-STD-883 allows a current density of less than 2.0E+05 A/cm^2 if the step coverage is 30% minimum for a geometry less than 1.5 μm. With this current density limit no electromigration problems are predicted assuming nominal operating conditions. The current density calculations done for the 2.0-μm technology showed the worst case for a single contact is 1.06E+05 A/cm^2 with 23.5% step coverage. This does not meet MIL-STD-883 but can be waived for some noncritical applications if the operating temperature is less than 90°C. The assumption being that by ACTEL's design rules a single contact is limited to 1 mA for the internal transistors which are doing AC logic switching. Input and output transistors have multiple contacts for current sharing and were not an issue. The 2-μm process electromigration lifetime calculation approximates 10 years (at 125°C) and 70 years (at 90°C) for $ttf_{.01}$ with a 50% duty cycle. This is acceptable provided the 1-mA current limit assumption is valid. The 1.2-μm process has a current density of 2.89E+05 A/cm^2 (12.5% metal step coverage). The predicted life is 1.5 years (at 125°C) and 10 years (at 90°C). The scaled technology is more at risk unless operating temperatures are kept below 90°C. Note that $ttf_{.01}$ indicates that 1 single contact or via out of 10,000 will fail given a log-normal failure distribution.

1.4 RADIATION TOTAL DOSE

Total dose testing was done on the A1010 and A1020 (2.0-μm) devices. One reported result for total dose is 150 krads (Si) with no functional and no post-irradiation effects (PIE) on parametric failures within 7 days of biased anneal. Icc standby leakage, input leakage, and output leakage demonstrated recovery to specification limits, or better. Other total dose tests have reported up to 300 krads (Si) with no failures. There were no PIE evaluations with the higher exposures. Based on the small sample size tested the A1010/A1020 devices are assured to 100 krad (Si).

The A1020A (1.2 μm) has shown functional failures between 100 krad (Si) and 200 krad (Si). These devices have shown recovery of the dynamic operating leakage current within 24 hr of anneal after 200 krad (Si) exposure.

The A1280 (1.2 μm) had functional failures at 5 krad (Si), 20 krad (Si), and 70 krad (Si) at 0 hr of post-irradiation testing. Functional recovery varied from 1 hr with ambient anneal to 24 hr with temperature anneal. Icc static leakage reached levels as high as 150 mA after irradiation with 125°C anneal. It is fair to state that the 1.2-μm device total dose results are less conclusive

than those for the 2.0-μm devices, and more radiation characterization is needed. It appears at this time that the A1280 does not have much TID tolerance beyond a few krads.

1.5 SINGLE EVENT EFFECTS

The ACTEL A1010/A1020 (2.0-μm technology) and A1020A (1.2-μm technology) were characterized for SEE. A ripple counter was configured by utilizing a number of ACTEL macro's and I/O's. The devices were bombarded with different heavy ion beams at variable flux. The devices exhibited no latchup at LET ≤ 120 MeV/(mg/cm^2). The upsets have been detected at LET ≥ 22 MeV/(mg/cm^2). The asymptotic cross section reported by APL was 2.3 x 10^{-6} cm^2/bit. The number reported by Aerospace Corporation was 1 x 10^{-4} cm^2/bit.

Another test of the 2-μm technology parts using a multiple twisted ring counter containing up to 100 vulnerable bits showed an upset threshold at LET ≥ 15 MeV/(mg/cm^2). These results were consistent at 100°C. It should be noted that the 2-μm technology uses only C-modules and this explains why the SEU performance is more consistent.

The ACTEL A1280 (1.2-μm technology) was evaluated using C-modules and S-modules. The measured effective LET is > 15 MeV/(mg/cm^2) for the C-module and < 5 MeV/(mg/cm^2) for the S-module. It is fair to conclude that designs using the A1280 will have lower LET thresholds compared to those using A1010/A1020. This limitation is the result of the S-modules.

1.6 ELECTRICAL CHARACTERIZATION AND LIFE TEST

The ACTEL 1020 was put on life test at T=125°C and Vcc=5.0 V. It successfully passed functional and parametric testing after 2000 hr. Some AC tests such as TPLH and TPHL failed the 5-V test limit marginally on select pins. These AC failures may possibly be attributed to test setup or fixture problems. An example of electrical characterization tests performed for the life tests is given in Subsection 2.5.

The ACTEL 1280 was put on life test at T=125°C and Vcc=5.0 V. It successfully passed functional and parametric testing after 500 hr. The units were put back on test but further results were not available for publication of this report. An example of electrical characterization tests for life test is given in Subsection 3.5.

The ACTEL 1020A was put on life test at T=175°C and Vcc =5.75 V. It successfully passed functional testing after 2000 hr. It was shown that one parametric test (IOL) exhibited a delta of between 12% and 18% of the original reading. This occurred on the majority of units and

most device pins tested for IOL. All other parametrics tested demonstrated less than 5% change throughout the life test. There was no failure analysis done on these parts to determine the apparent cause of the IOL drift. Graphs for the IOL test characterization can be found in Subsection 4.2.

1.7 CONCLUSIONS

The objective of evaluating the ACTEL FPGA's (manufactured by Matsushita) was to determine their present capability and future potential for space applications. The ACTEL technology and FPGA architecture are among many available to the aerospace community. However the ACTEL products were chosen as having more radiation tolerance in earlier investigations. Therefore a more thorough review and evaluation was warranted and now successfully completed by the aerospace community.

Two important requirements for space application are product reliability and quality. To evaluate these, there was examination of the manufacturing process using destructive physical analysis methods. In addition product life tests were conducted. The life tests and DPA evaluation were directed toward giving insight into whether the technology and product could meet the stringent standards necessary for space applications. All space projects and designs will have different part standards and requirements. But some minimum level of reliability must be assured to be deemed acceptable by the aerospace community. The one concern as a result of the DPA is the poor quality of metal step coverage. The A1010/A1020 (2 μm) is acceptable provided a 20% minimum step coverage in contacts and vias is met by the manufacturer and the application temperature is limited to 90°C. The A1280 (1.2 μm) and the A1020A (1.2 μm) are not recommended at this time because mission lifetime is jeopardized due to possible electromigration. Product life testing also showed evidence that some parameters may change. To insure against these changes a delta criteria is recommended as part of the screening flow or life tests.

The radiation data collectively for the A1010/A1020 show the product to have an acceptable TID tolerance for some space applications. The total dose achieved without any hard failures is at or slightly above 100 krads (Si). SEU LET thresholds appear to be in the 15 to 25 MeV/(mg/cm^2) range. There was no latchup observed for LET ≤ 120 MeV/(mg/cm^2).

The A1280 is more vulnerable to SEU, because by design it is comprised of C-modules and S-modules. The S-module LET threshold is less than 5 MeV/(mg/cm^2). The total dose for the A1280 is at 5 krads (Si), significantly less than that for the A1010/A1020. Further study of the A1280 is needed to understand its limited performance.

In summary we hope this report provides useful information to all space application users. It was through the cooperation of all who participated and those who contributed information that a much better understanding of the FPGA's performance as a radiation hard and reliable device has been achieved.

1.8 ACTEL FPGA REPORTED RESULTS

	JPL	HAC	TRW	APL	GE ASTRO	AEROSPACE	COMMENTS
Metal Step Coverage							
A1010/A1020	23.5% in via						
A1280	12.5% in via						
A1020A			4.5-20% (contact/via)				
Current Density							
A1010/A1020	1.06E+05 A/cm^2						
A1280	2.89E+05 A/cm^2						
A1020A			1.10E+05 A/cm^2				
Total Dose							
A1010/A1020				(a) 300 krads (Si)	150 krads (Si)		
A1280		(f) 20 krads (Si)		5 krads (Si)			
A1020A			(b) 100 krads (Si)	100 krads (Si)			
SEU (LETth)							
A1010/A1020-C cell				(d) 25 Mev-cm^2/mg			
A1280-S cell						5 Mev-cm^2/mg	Room to 100°C
A1010/A1020-C cell						25 Mev-cm^2/mg	Room to 100°C
A1280-C cell						23 Mev-cm^2/mg	Room to 100°C
A1020A-C cell				(d) 22 Mev-cm^2/mg			
LATCHUP							
A1010/A1020						Null @ 15-120 LET	Room to 100°C
A1280						Null @ 15-120 LET	Room to 100°C
Upset Rate							
A1010/A1020						3E-7 upset/bit-day	geosynchronous orbit
A1280-S				1E-6 errors/bit-day		1E-6 upset/bit-day	geosynchronous orbit
A1280-C				1E-7 errors/bit-day		1E-7 upset/bit-day	geosynchronous orbit
Life Test(pass)							
A1020A			44/44 @ 2000 hrs				IOL drift recorded was 12-18%
A1020	10/10 @ 2000 hrs						
A1280	10/10 @ 500 hrs						Marginal AC performance
Life Prediction							
A1020 (2 micron)	(c) 16.2yrs @ 130°C						Ea=0.63 ev (electromigration)
A1020A (1.2 micron)			1.9yrs @ 130°C				Ea=0.63 ev (electromigration)
A1280 (1.2 micron)	(c) 2.2yrs @ 130°C						Ea=0.63 ev (electromigration)
Dose Rate							
A1280 (1.2 micron)			5.5E8 rads/sec				Output Transients
A1280 (1.2 micron)			1E9 rads/sec				Permanent Data Errors
A1020 (2 micron)			(e) 2E9 rads/sec				Output Transients

notes

(a) @13 rad/sec
(b) @79 rad/sec
(c) for t50 single critical contact failure
(d) cross-section = 2.3E-8 cm^2/bit
(e) reported by Magnavox Electronics Co
(f) 5/5 nonfunctional @ 0-hr post irradiation
@20 krad Idd = 150 ma max(125°C; 48 hrs)

SECTION 2.0
Actel 1020 (2 μm)

SECTION 2.1
Radiation Data Total Dose

GE ASTRO SPACE SUMMARY REPORT
RADIATION TOTAL DOSE GRAPHS

PRODUCT: CMOS FIELD PROGRAMMABLE GATE ARRAY

MANUFACTURING BY: MATSUSHITA

DEVICE: ACT1010(1020) 2 MICRON

EVALUATED BY: GE ASTRO SPACE

REF: INTERNAL REPORT(J.M.LOMAN)"RADIATION TESTING OF ACT1010 PROGRAMMABLE GATE ARRAYS"

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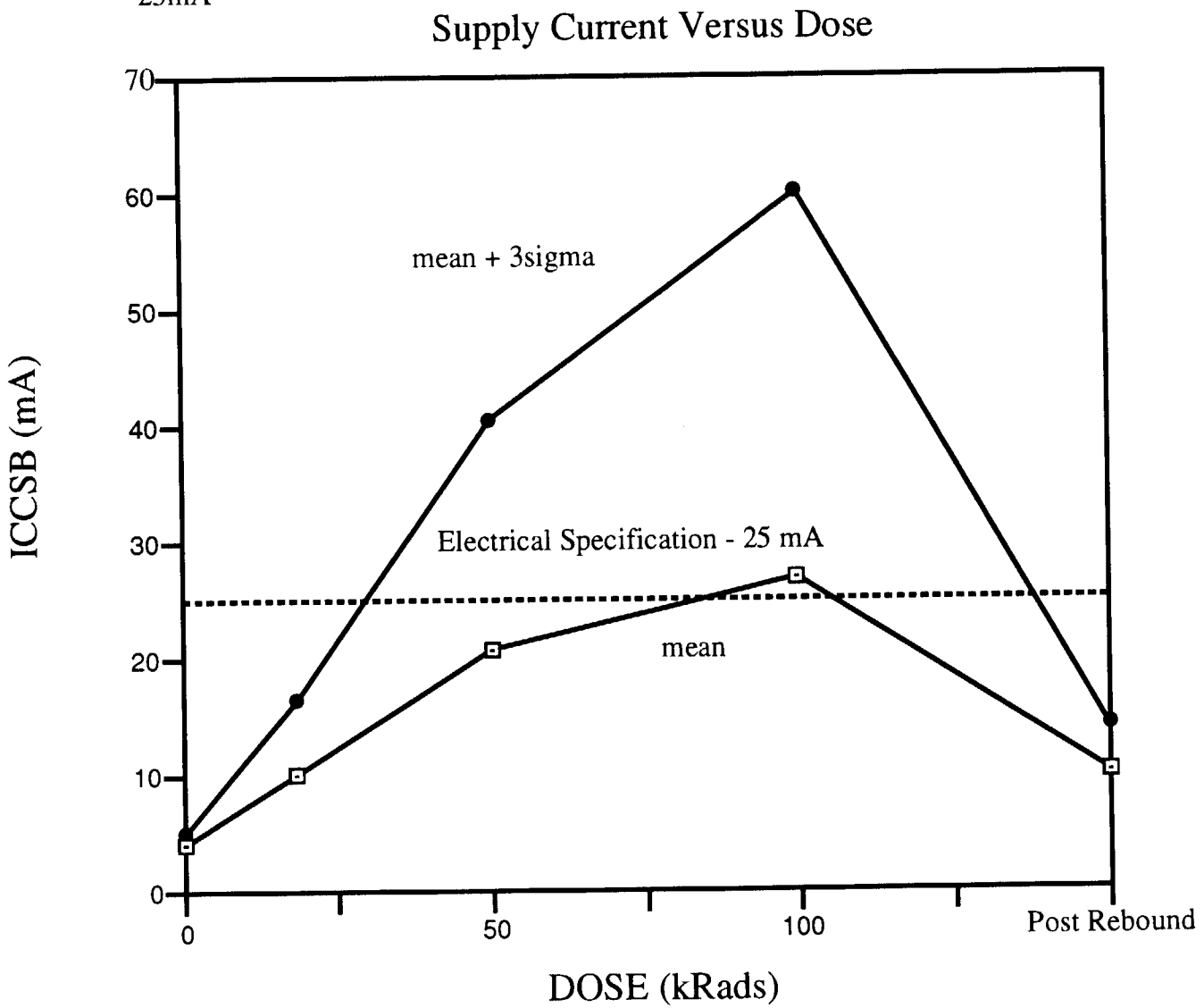
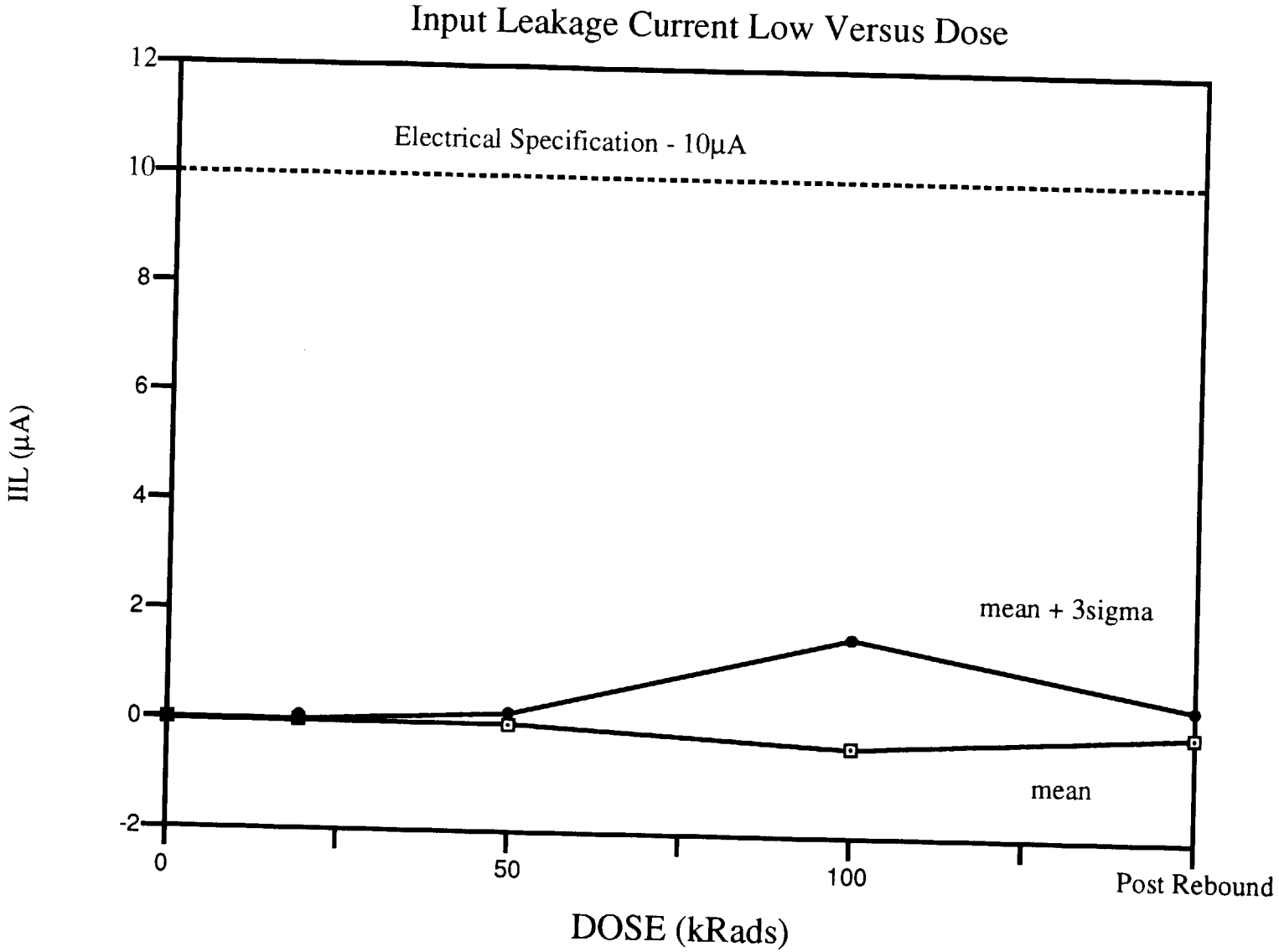
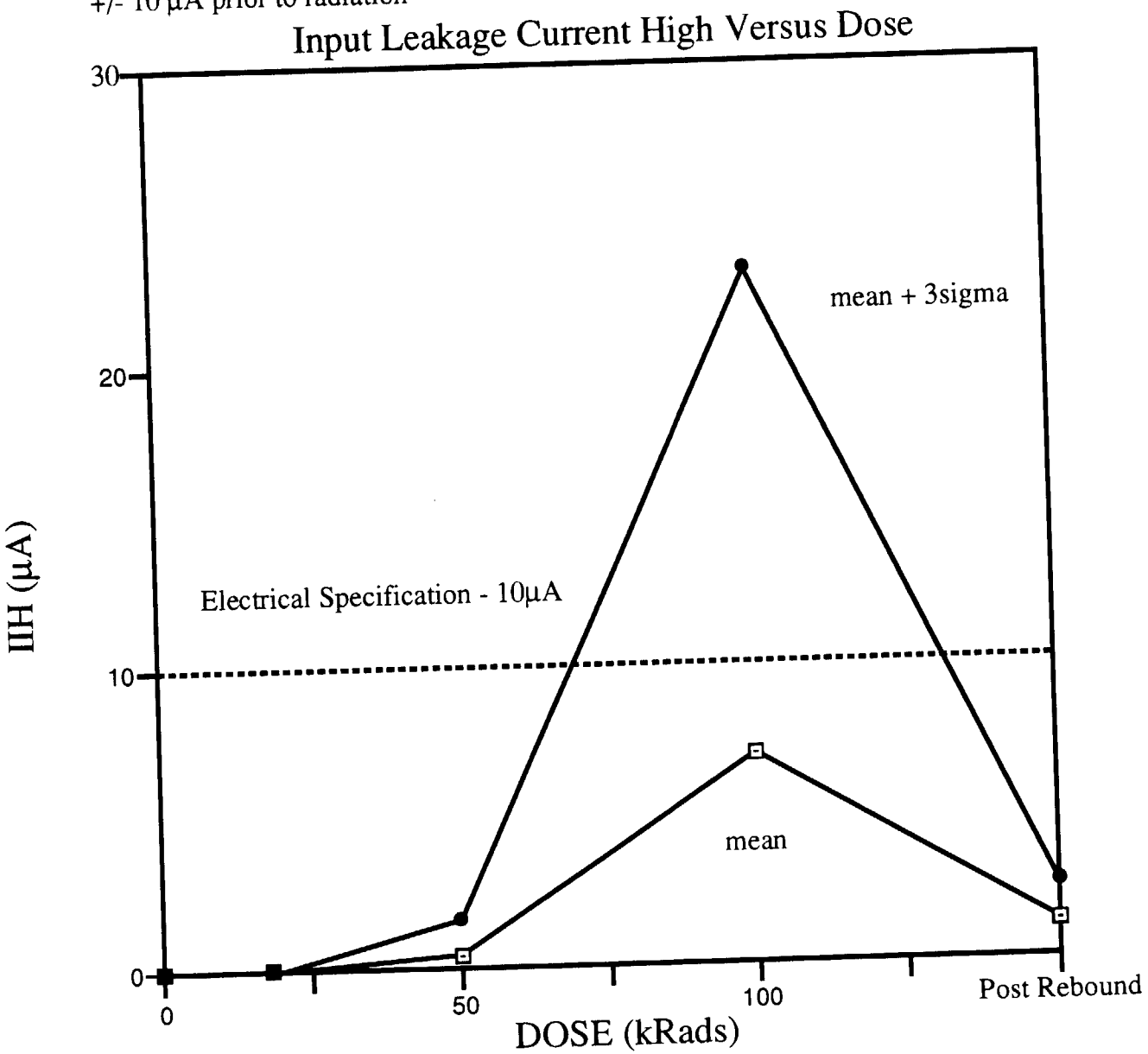
ACTEL Gate Array Supply Current Performance as a Function of Total Dose. The parametric mean and (mean + 3sigma) are plotted on the curve. The electrical specification from the ACTEL catalog was specified at a maximum of 25mA



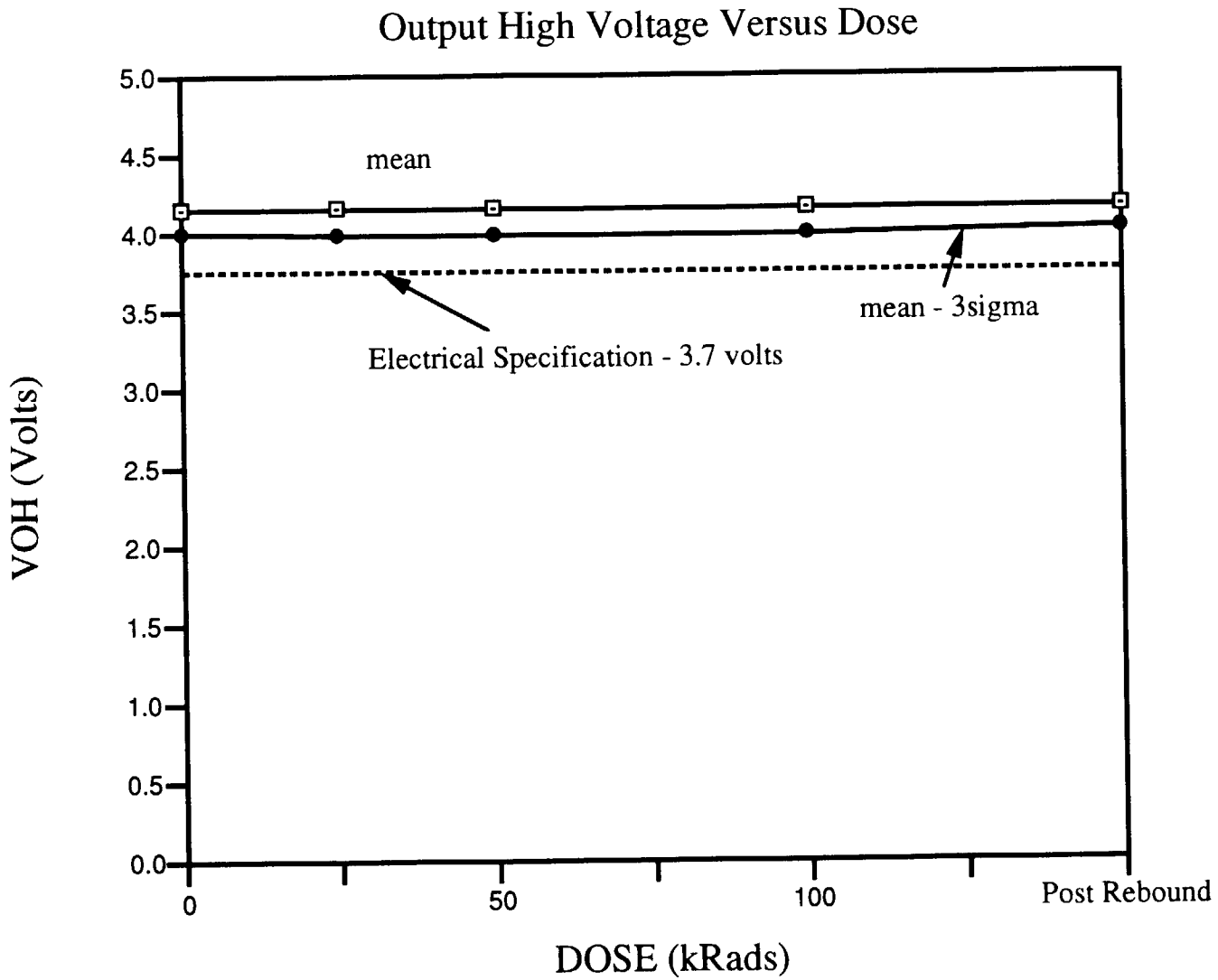
ACTEL Gate Array Input Leakage Current Low (IIL) as a Function of Total Dose. The electrical specification for IIL in the ACTEL catalog is between +/- 10 μA prior to radiation



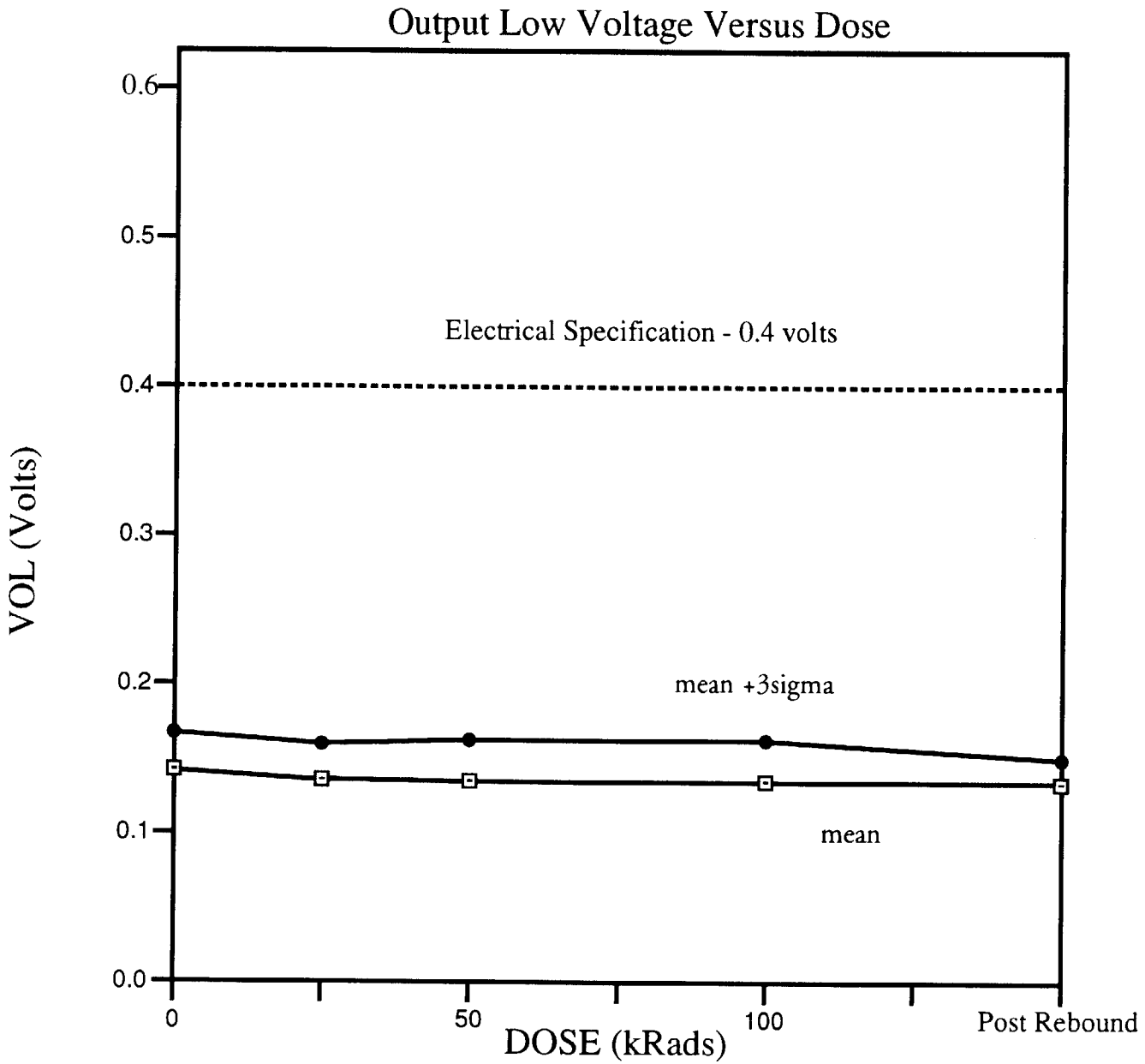
ACTEL Gate Array Input Leakage Current High (IIH) as a Function of Total Dose. The electrical specification for IIH in the ACTEL catalog is between +/- 10 µA prior to radiation



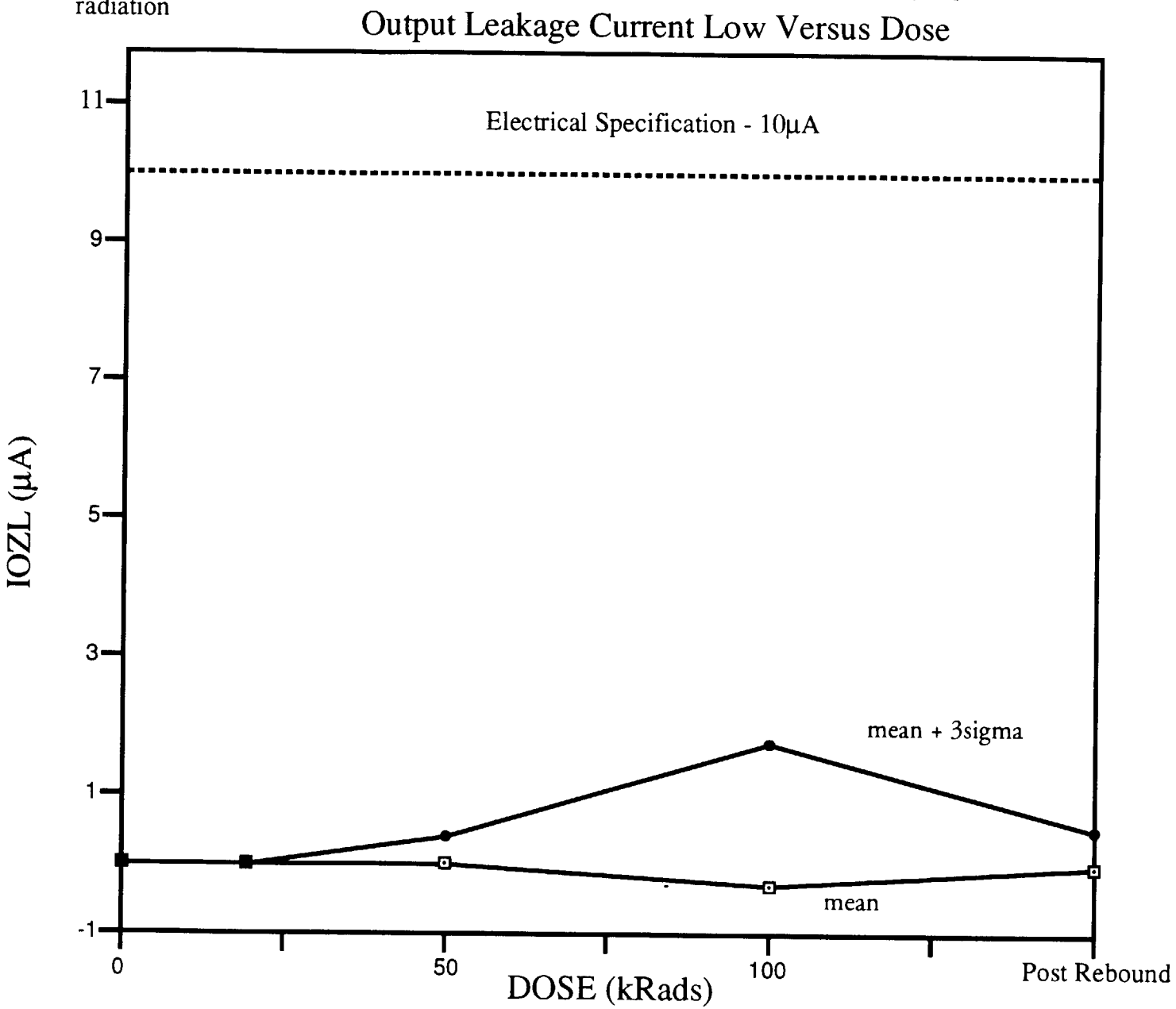
ACTEL Gate Array Output Voltage High (VOH) as a Function of Total Dose. The electrical specification for VOH in the ACTEL catalog is a minimum of 3.7 volts.



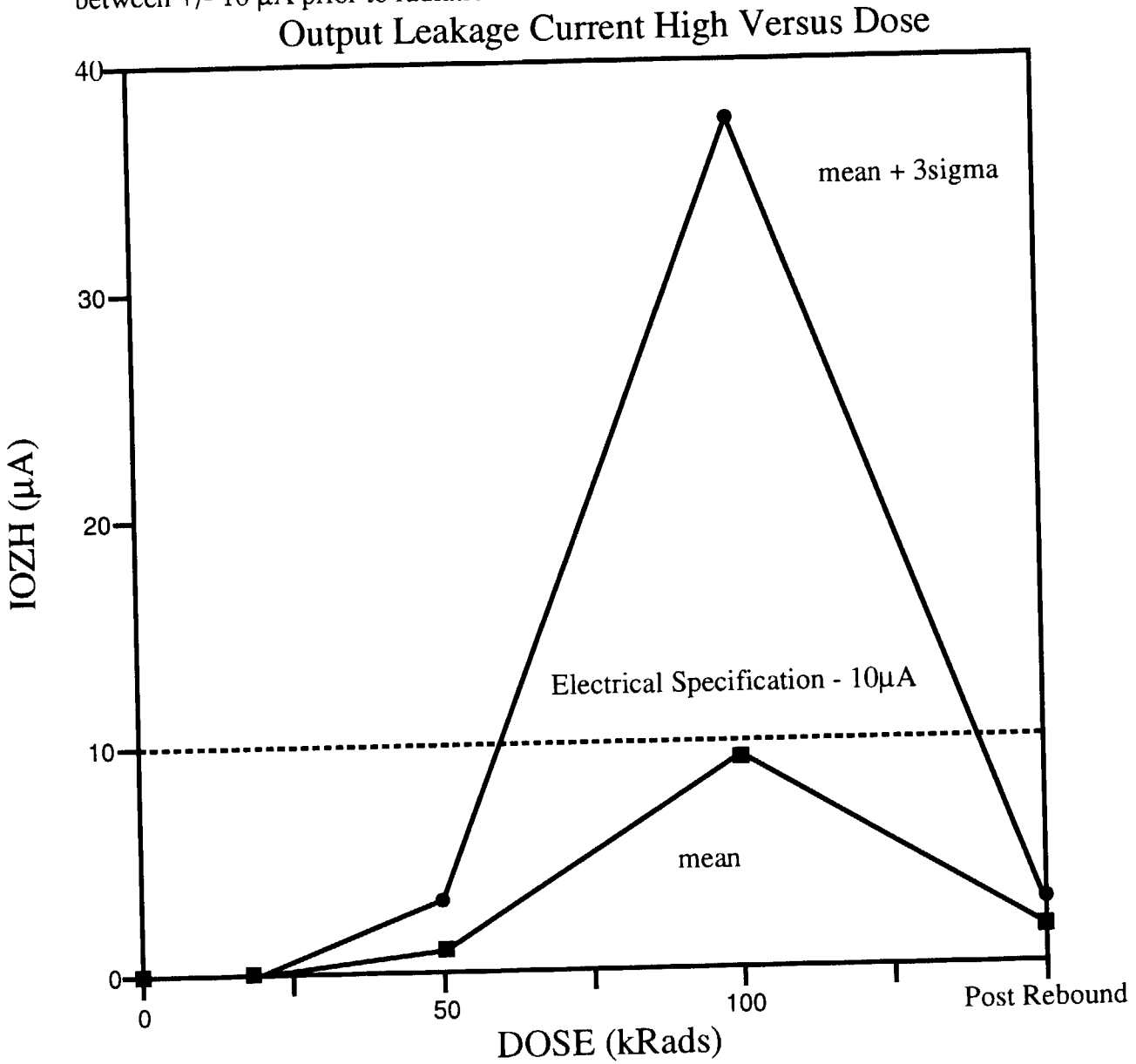
ACTEL Gate Array Output Voltage Low (VOL) as a Function of Total Dose. The electrical specification for VOL in the ACTEL catalog is a maximum of 0.4 volts.



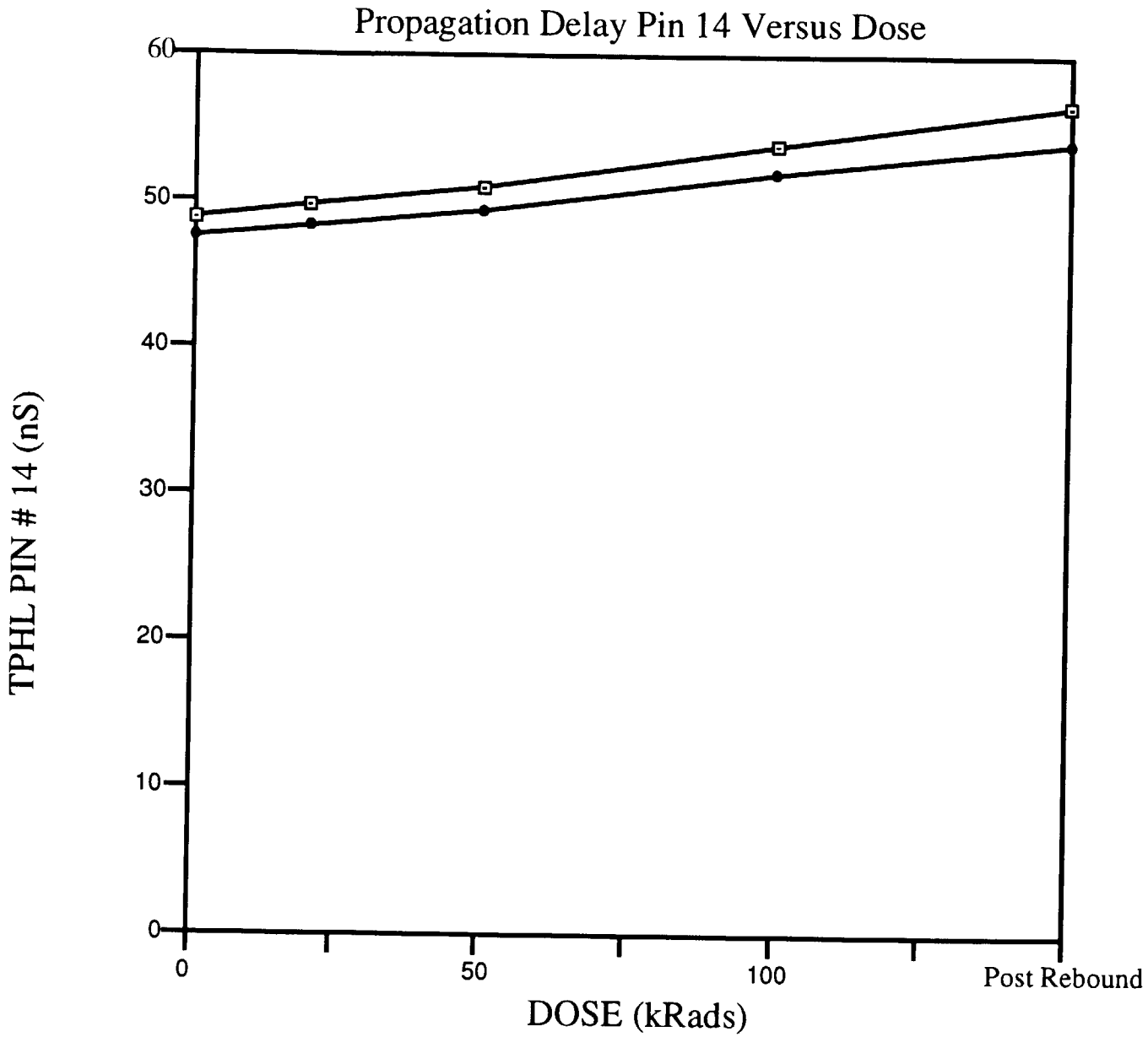
ACTEL Gate Array Output Leakage Current Low (IOZL) as a Function of Total Dose. The electrical specification for IOZL in the ACTEL catalog is between +/- 10 µA prior to radiation



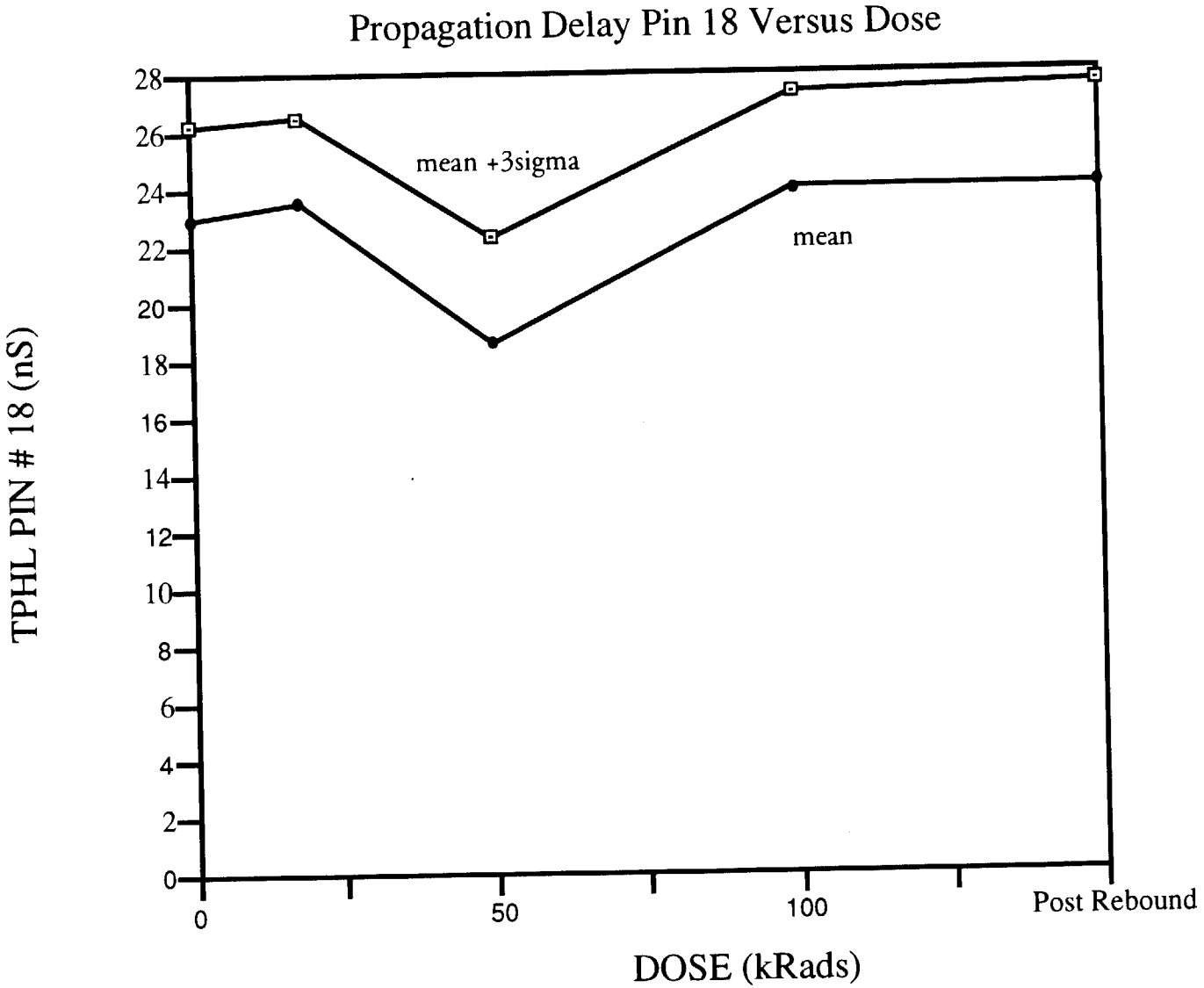
ACTEL Gate Array Output Leakage Current High (IOZH) as a Function of Total Dose. The electrical specification for IOZH in the ACTEL catalog is between +/- 10 µA prior to radiation



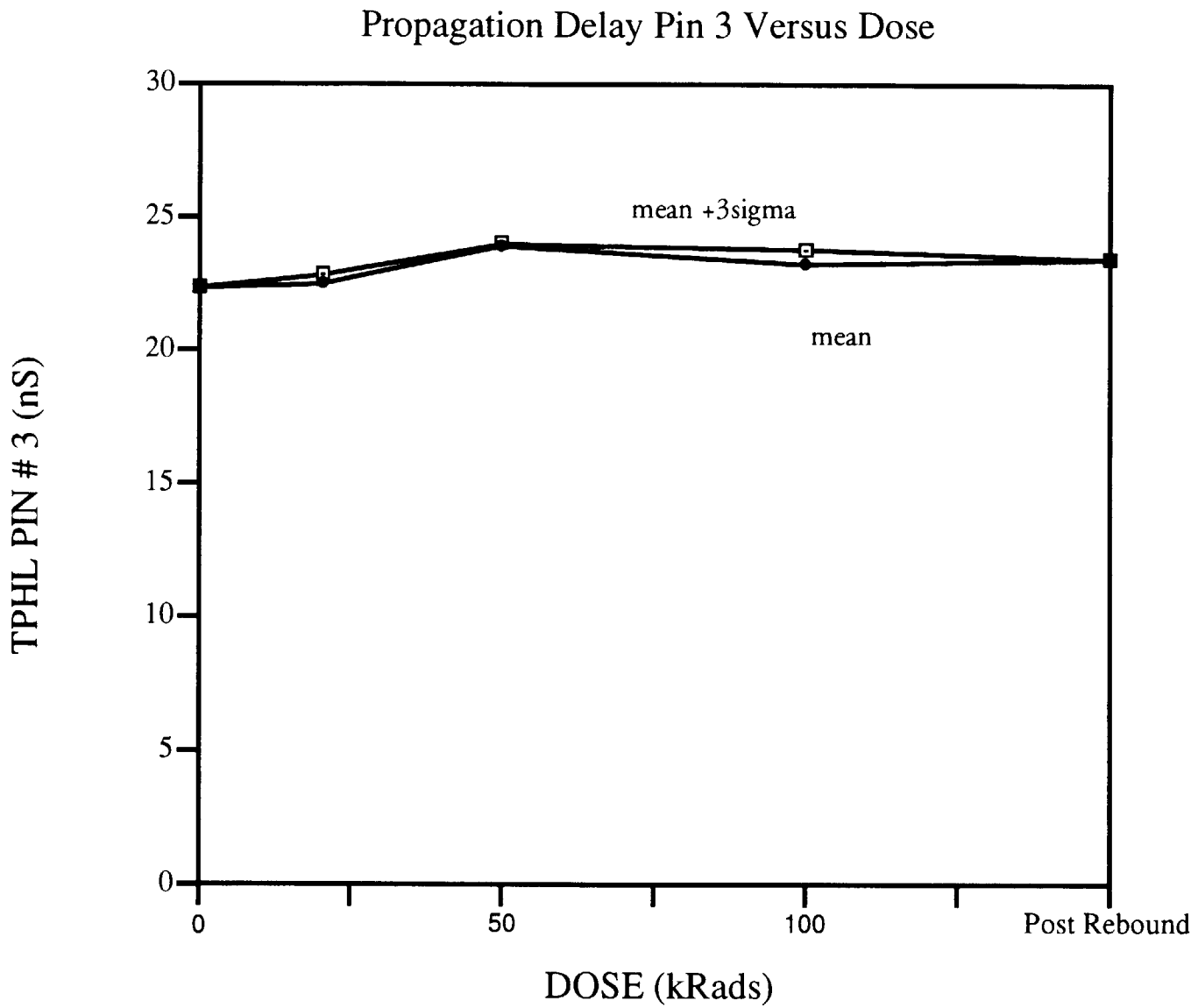
ACTEL Gate Array Propagation Delay High to Low - Pin #14 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



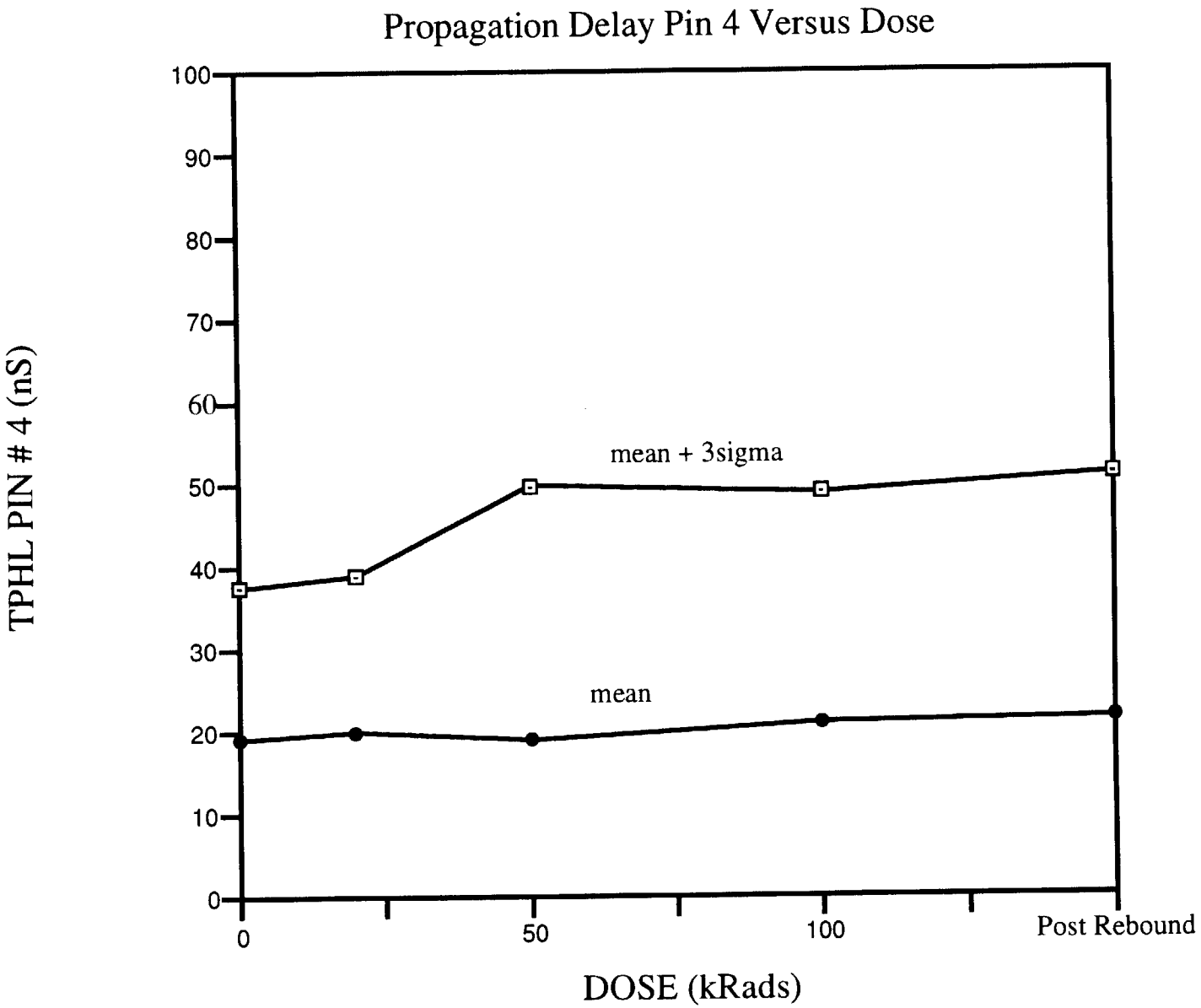
ACTEL Gate Array Propagation Delay High to Low - Pin #18 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



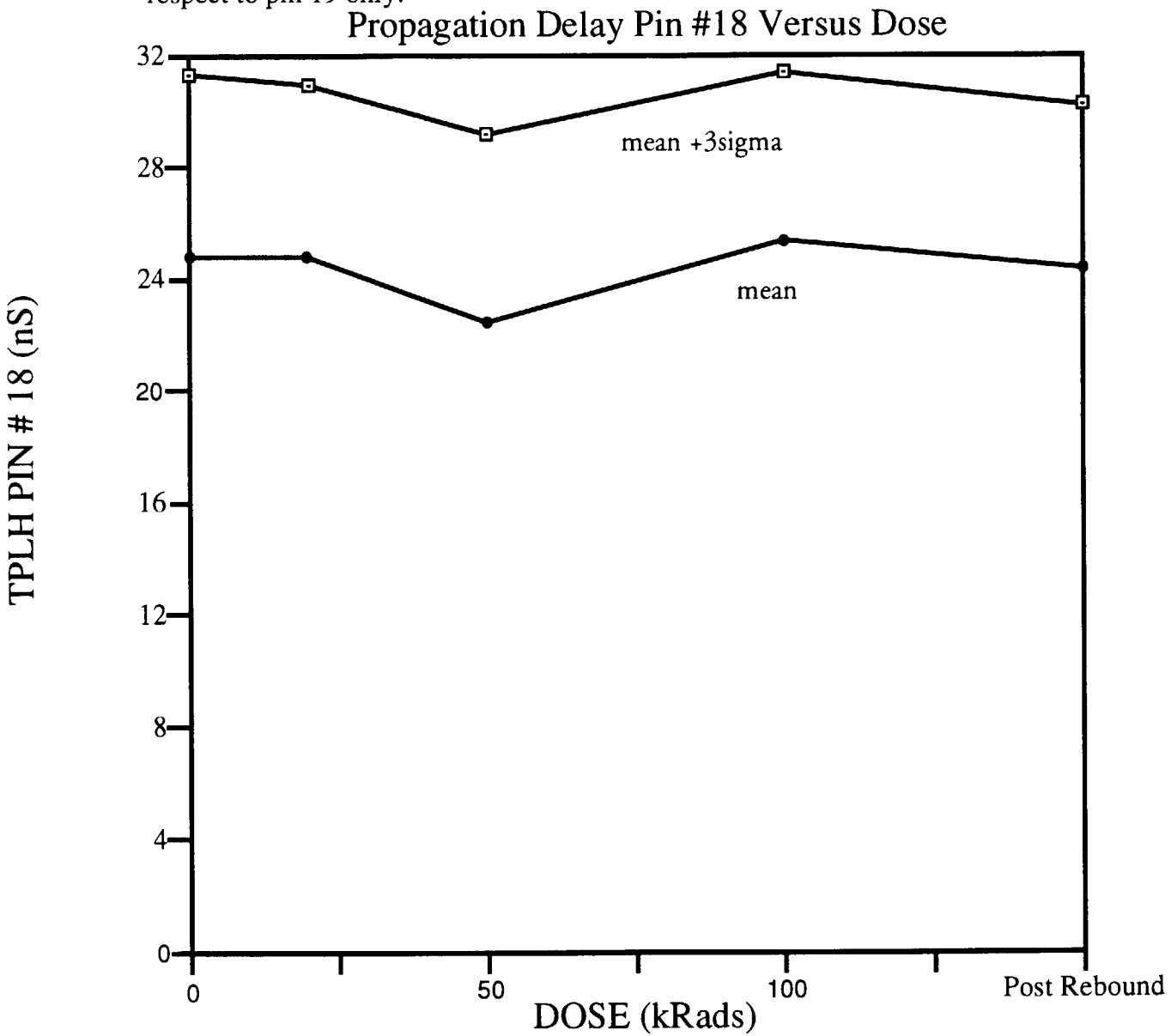
ACTEL Gate Array Propagation Delay High to Low - Pin #3 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



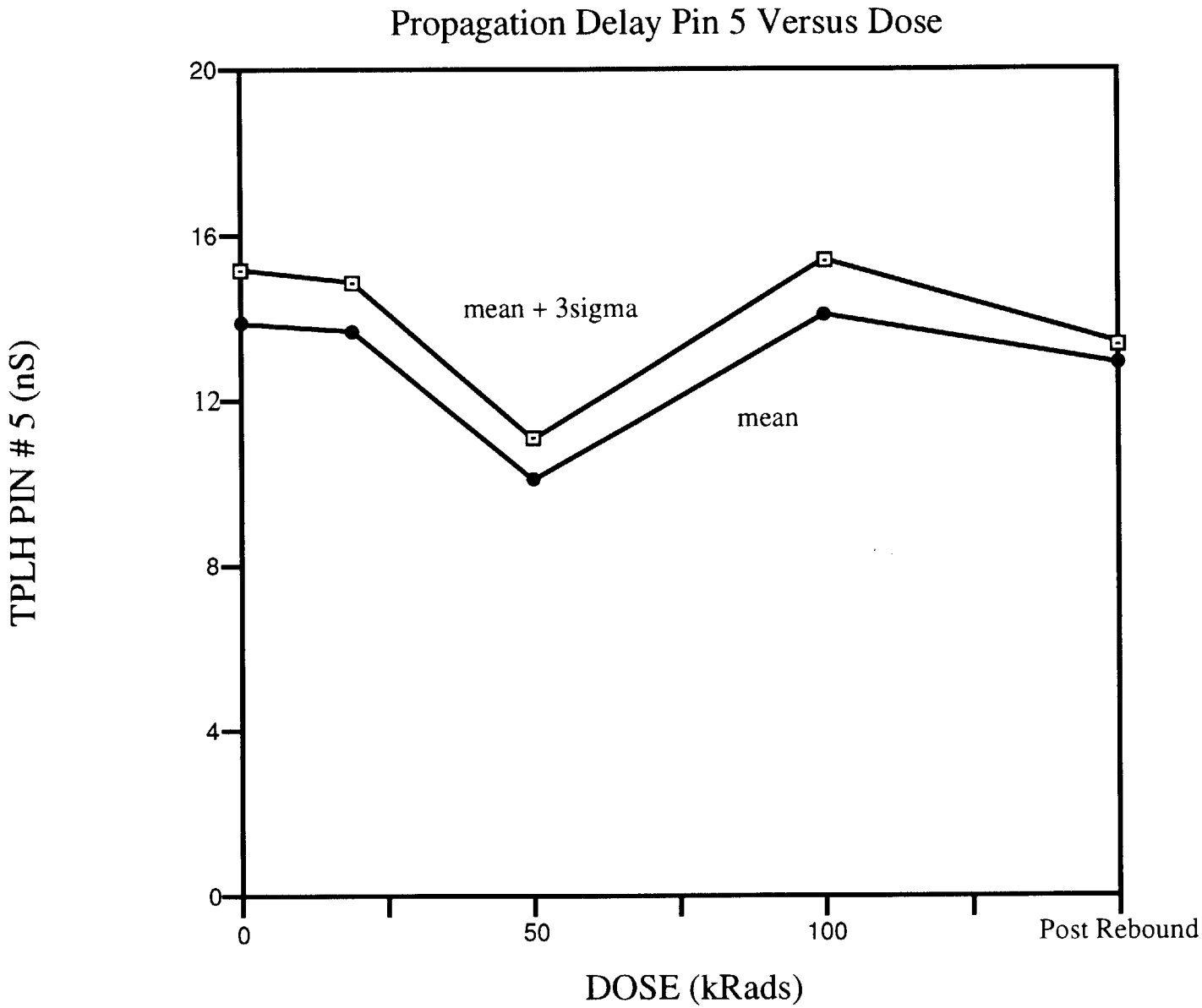
ACTEL Gate Array Propagation Delay High to Low - Pin #4 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



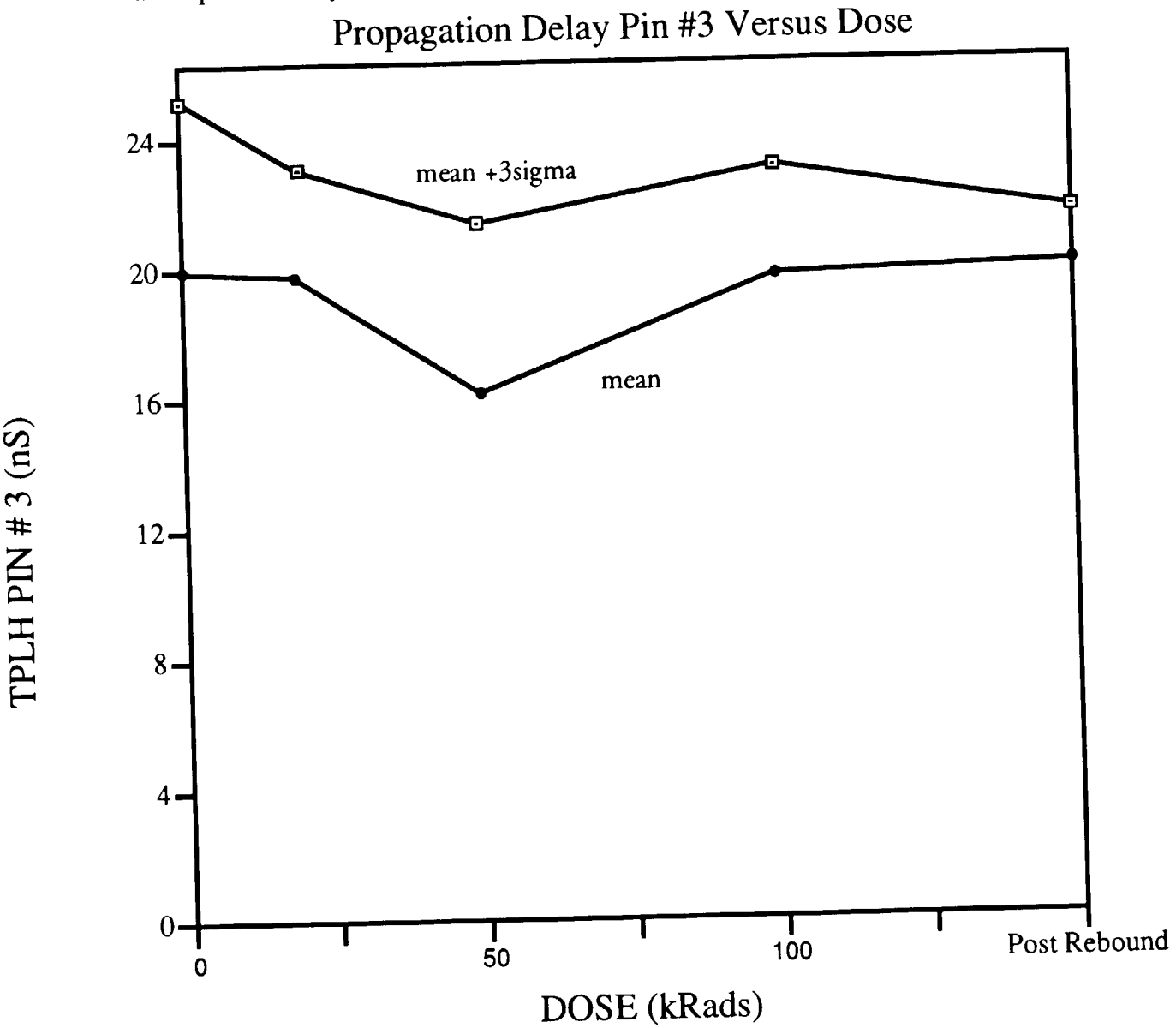
ACTEL Gate Array Propagation Delay Low to High - Pin #18 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma. This propagation delay time is with respect to pin 19 only.



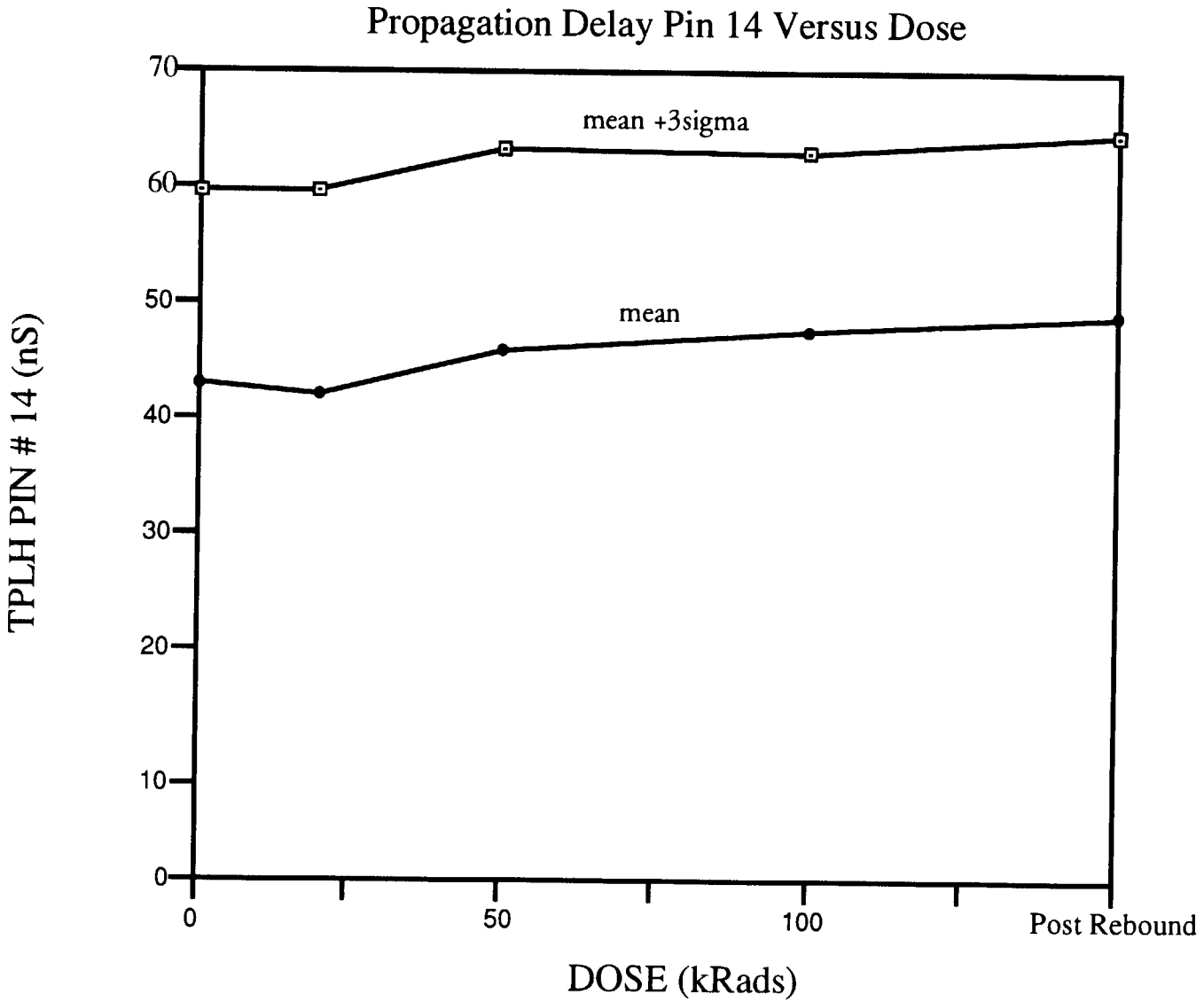
ACTEL Gate Array Propagation Delay Low to High - Pin #5 plotted as a function of Total Dose. The worst cases variations on the propagation delay time are represented by the mean +3sigma.



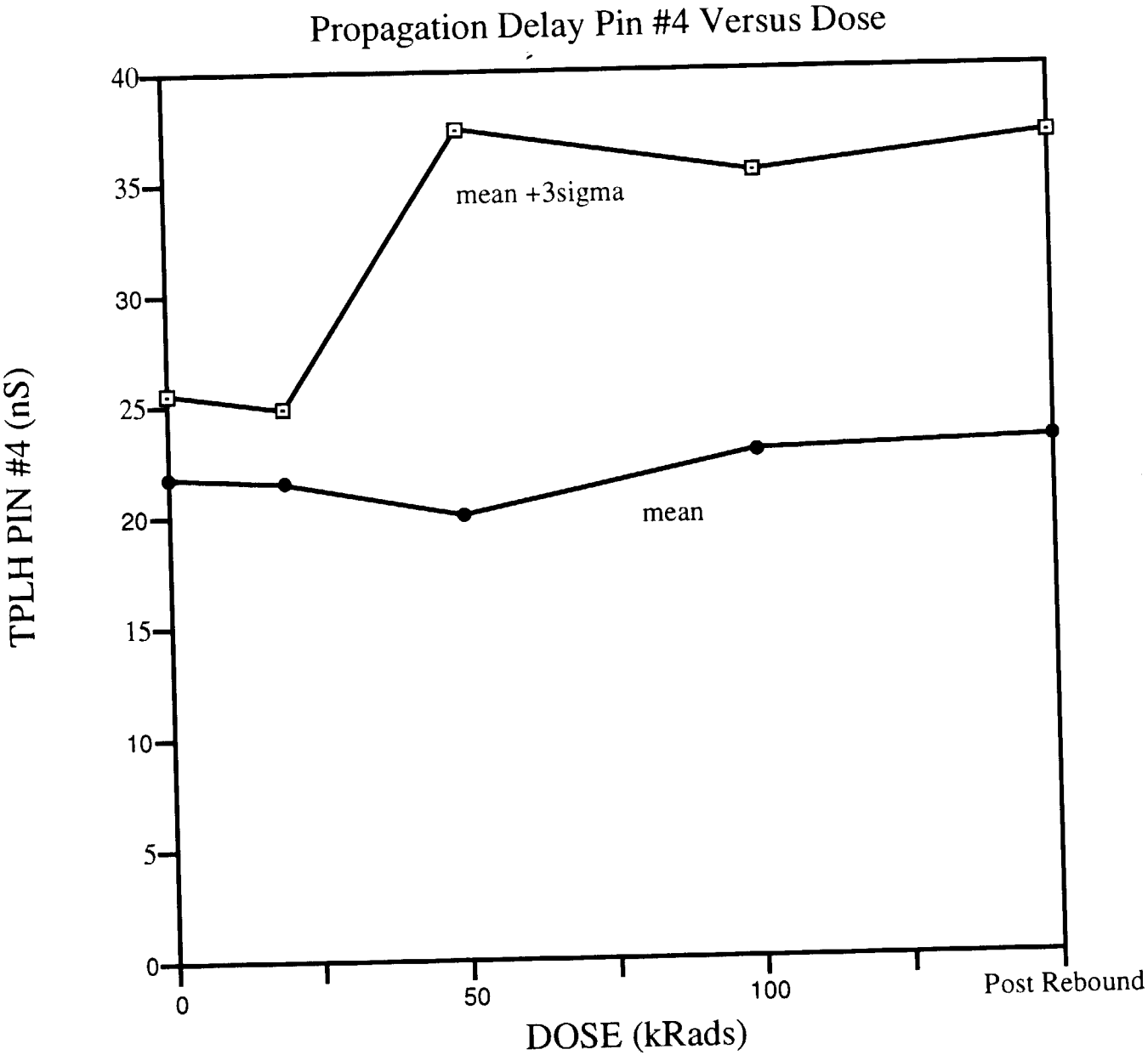
ACTEL Gate Array Propagation Delay Low to High - Pin #3 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



ACTEL Gate Array Propagation Delay Low to High - Pin #14 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



ACTEL Gate Array Propagation Delay Low to High - Pin #14 plotted as a function of Total Dose. The worst case variations on the propagation delay time are represented by the mean +3sigma.



SECTION 2.2
Radiation Data SEU

AEROSPACE CORPORATION SUMMARY REPORT

PRODUCT: CMOS FIELD PROGRAMMABLE GATE ARRAY
MANUFACTURING BY: MATSUSHITA
DEVICE: ACT1010/ACT1020 (2.0 micron); ACT1280 (1.2 micron)
EVALUATED BY: AEROSPACE CORPORATION
Ref. (1)Single Event Effects Testing Report by R.Koga
Ref. (2)Single Event Upset and Latchup Susceptibilities of Actel A1280 CMOS Field Programmable Gate Array Report by R.Koga & S.J.Hansel

EVALUATIONS:

A1280 SINGLE EVENT UPSET (SEU) and LATCHUP SUSCEPTIBILITY

Data was taken on four devices each of which was programmed using four sequential ring counters and four combinatorial ring counters. Each device module was programmed as a multiple twisted ring counter using 60 D-type flip-flops. All programming was accomplished with antifuse elements. The programming was performed by ACTEL.

The test measurement was accomplished by by comparing the correct output signature of an unexposed device to the device that is exposed to the ion beam. Each device tested is exposed to a number of cycles while a sufficient number of output errors is accumulated and recorded. During exposure the power supply current was also monitored to detect latchup. SEU and latchup measurements were taken at room temperature and at 100°C.

Test results show that null latchup results were measured at the effective LET's ranging from 15 to 120 Mev/(mg/cm2). The SEU measurements were taken and plotted as (cm2/240 flip-flops) vs LET[MeV/(mg/cm2)]; See figure 3. Examination of the data shows that C-modules are less vulnerable than S-modues for SEU. At 100°C the results are identical.

A1010/A1020 SINGLE EVENT UPSET (SEU) and LATCHUP SUSCEPTIBILITY

The parts evaluated for SEU were exposed to Xe(603 MeV), Kr(380 MeV),Cu(290 MeV), and Ar (180 MeV) ion beams. They were programmed as multiple twisted ring counters each of which was 10 bits long. The A1010 and A1020 were programmed to hold four and five ring counters which contained 40 and 50 vulnerable bits.

The test measurement was done similarly as described for the A1280.

Test results show that null latchup results were measured at the effective LET's ranging from 15 to 120 Mev/(mg/cm2). The SEU measurements were taken and plotted as (cm2/ 40 or 50 flip-flops) vs LET[MeV/(mg/cm2)]. From the data it is seen that the A1010 and A1020 have similar susceptibilities. The test results at 80°C and 100°C are nearly identical to those at room temperature. Null latchup were measured at effective LETs ranging from 15 to 120 MeV/(mg/cm2). See figure 4 and 5.

Post SEU testing of antifuses at 100°C revealed some errors. However it is speculated these errors were the result of using commercial devices rated and tested to 70°C. There was also some indication of mishandling the parts after SEU testing.

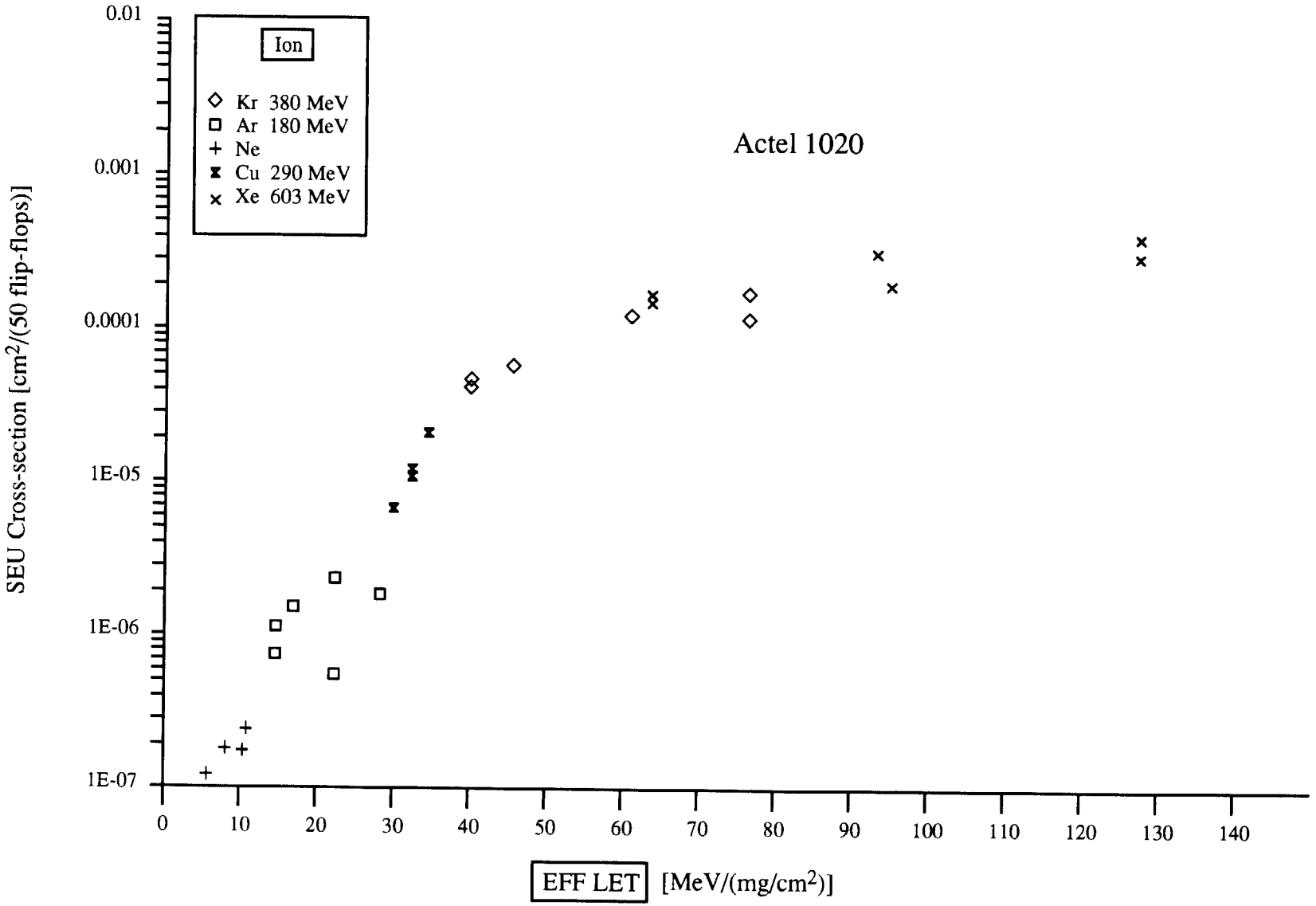


Figure 4. SEU Test Results for ACT1020

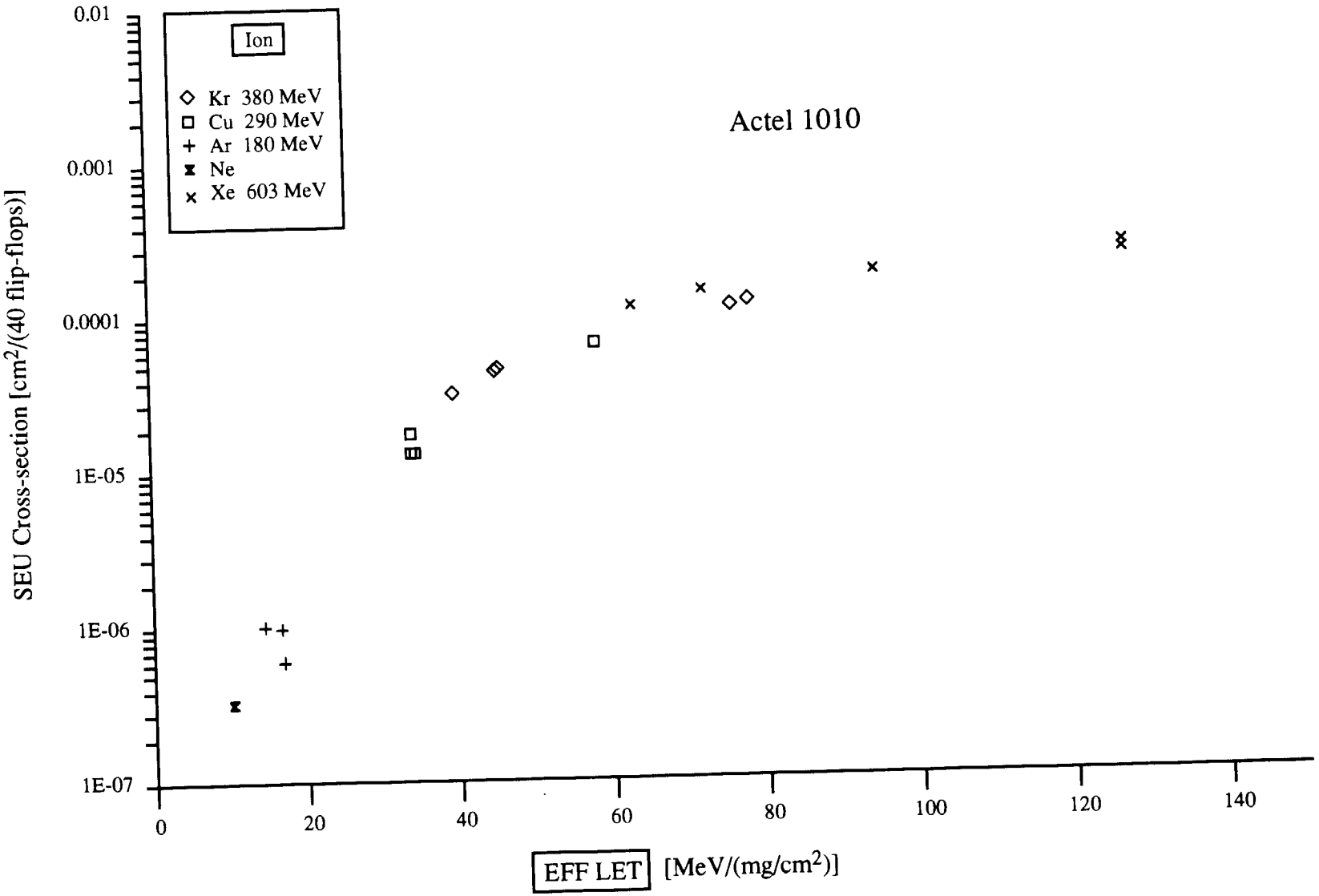


Figure 5. SEU Test Results for ACT1010

APPLIED PHYSICS LABORATORY SUMMARY REPORT

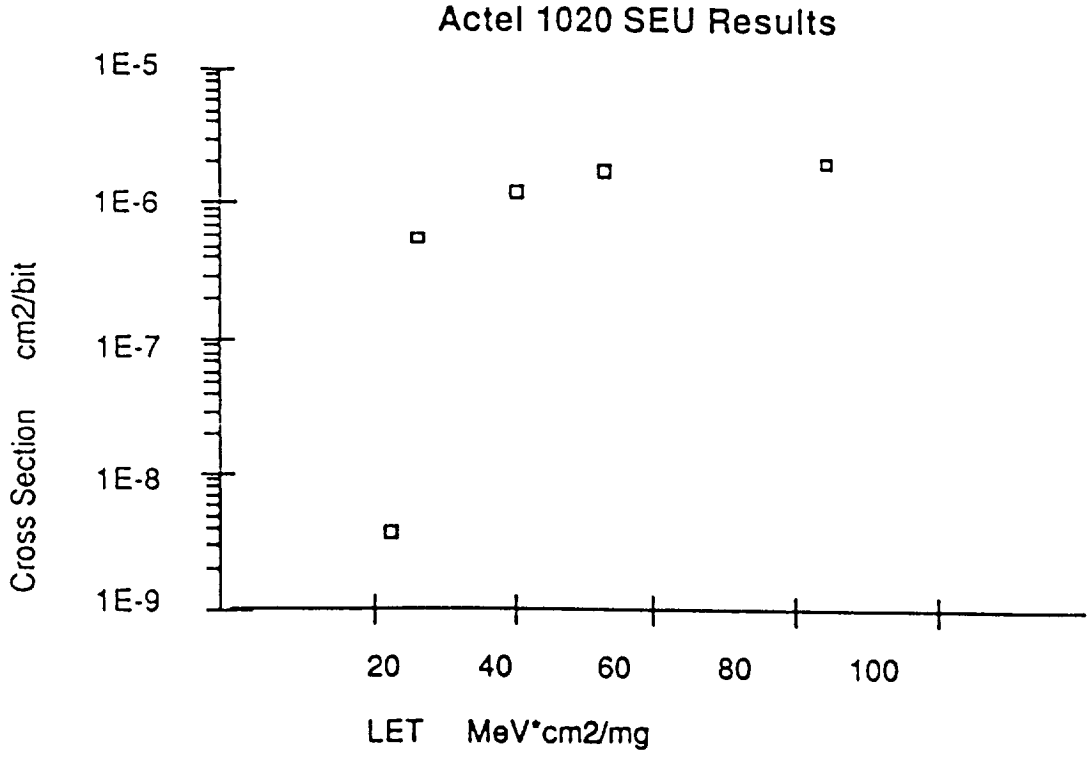
PRODUCT: CMOS FIELD PROGRAMMABLE GATE ARRAY
MANUFACTURING BY: MATSUSHITA
DEVICE: ACT1020 (2.0 micron)and ACT1020A(1.2 micron)
EVALUATED BY: APPLIED PHYSICS LABORTORY
Ref: Internal Report "Electrical and Radiation Qualification Methods for Field Programmable Gate Arrays in Space Applications"

EVALUATIONS:

SINGLE EVENT UPSET (SEU)

SEU sensitivity for the original 1020 and the scaled version (1020A) were evaluated for cross-sections. Parts evaluated were programmed using 547 logic modules in a chain of 262 flip-flops. Detection and counting would result if any upset would occur in the chain. After an occurence a reset would be initiated.

Test results for both versions were consistent. The asymptotic cross-section for both versions was 2.3 x 10E-6 cm2/bit. The threshold Linear Energy Transfer for the 1020 was 25 MeV-cm2/mg while the threshold for the scaled version was about 22 MeV-cm2/mg.



SECTION 2.3
DPA Product Analysis/Step Coverage

PARTS INFORMATION PROGRAM

ELECTRONIC PARTS RELIABILITY SECTION

PIP No. 304

JPL
Jet Propulsion Laboratory
California Institute of Technology

DATE 7 April 1992

SUBJECT: Preliminary Product Analysis (PA) of ACT-1020B CMOS Field Programmable Gate Array (FPGA) device manufactured by Actel Corp.

SUMMARY: One ACT-1020B FPGA CMOS device in pin grid array (PGA) package was submitted to the JPL LSI group for destructive product analysis. This PA effort is a part of the JPL/NASA Quality Assurance Program for selection and qualification of field programmable logic array devices considered for use in flight hardware systems for the Earth Observation System (EOS) and Cassini Missions. The evaluation results provide initial insight into the quality of FPGA Si-chip materials structures, and identify antifuse oxide/nitride/oxide (ONO) dielectric and poly structure of programmable logic cell with fused and intact ONO patterns, as shown in Figures 7d, 11b and 12b.

The FPGA chip top passivation utilizes two-level dielectric of nitride on SiO_2. The chip has two-level (Si- and cu-doped aluminum) metal interconnections; metal-2 interconnects with metal-1, and metal-1 interfaces with poly and Si contacts. The chip intrametal dielectric is a two-layer (unplanarized) Spin-on Oxide (SOG) on Low Temperature Oxide (LTO). The chip two-pattern polysilicon is; gate-poly on thin gate oxide, and PAL-poly on ONO. All poly patterns and thick field oxide are covered by a thin nitride film prior to BPSG deposition. Local oxidation is used for thick field oxide lateral isolation of FPGA cells and MOS transistors. The device requires a single source 5.0 V supply. The attached manufacturer's data sheets provide detailed information on electrical and environmental functionality of the 1020B CMOS FPGA device.

SOURCE OF INFORMATION:

JPL LSI Engineering Group, Section 514, S. Suszko.

FOR ADDITIONAL INFORMATION CONTACT: Stefan Suszko **EXT:** 4-1716 or 4-7709

APPROVED: Group Supervisor - LSI Engineering Group

Overview of Package and FPGA Chip Optical and SEM Examinations:

Figures 1a through 12d are optical and scanning electron microscope (SEM) photo views, which, together with captions, provide detailed examples for identification and definition of FPGA 1020B Si-chip materials structures, their interface integrity, and dimensions. See Table I.

1) SEM Examination of Chip Laterally Exposed Metal Interconnections: Figures 2a through 4c show exposed metal-2 with good contact alignment to metal-1. Though there are unusual metal-2 step features over SOG and LTO dips above metal-1 contacts, these are not metal-2 to metal-1 contacts, as shown in Figures 2d, 3d, and 4c. These metal-2 steps only replicate unplanarized intrametal SOG and LTO over metal-1 contacts.

   Figures 5a through 6d are scanning electron microscope (SEM) photo views of exposed metal-2 and metal-1 interconnections showing contact patterns and step coverage (after removal of intrametal SOG and LTO).

   Figures 7a through 7d are SEM photo views of exposed MOS transistor cells with thin nitride film over field oxide, gate poly patterns, and programmable array cells (PAL) poly patterns, and exposed contacts to poly and Si (after removal of two-level metal and interlevel dielectrics).

2) SEM Examination of Two FPGA Chip Cross-Sectioned Segments: Figures 8a through 10b are SEM photo views which show cross-sectioned details of metal-2 to metal-1 contacts, and metal-1 to poly and Si contacts, and features of via cuts in BPSG for metal-1 contact interface to poly and Si.

   Figures 10c and 10d show identified details of poly gate length and thickness structure with sidewall oxide for L_{DD}, and effective channel length. A pattern of thin nitride film over poly oxide and field oxide is identified in Figure 10d.

   Figures 11a through 12d show cross-sectioned details of PAL-cell poly on ONO dielectric structure (at 0° and 90° cross-sectioned segments) with intact ONO between poly and Si, and with fused (programmed) poly to Si through 1000 Å thick ONO dielectric, (as in poly to Si buried contact).

   For dimensions of materials structures on Si, and Si-chip, see Table I.

Conclusions

Evaluation results of the Actel FPGA 1020B Si chip show evidence of metal-2 thinning in via step coverage to metal-1 contacts, with 0.25 μm

step coverage thickness, or 25% of nominal 1 μm thick metal-2 (Figure 8b). A similar thinning effect is also evidenced in metal-1 step coverage in BPSG aperture cuts to poly and Si contacts; with minimum metal-1 step coverage thickness of 0.2 μm or ≈30% of the 0.85 μm nominal thickness as shown in Figures 8c through 9d. The thickness quality of metal step coverage as shown in these figures does not meet the acceptance criteria of MIL-STD 883C.

However, reliability data may be acceptable to pass this metal step coverage in contacts for current density requirements according to MIL-M-38510, as calculated by Mike Sandor of JPL (Ref: JPL IOM 514-F-038-92, dated 2/14/92) Calculation of Current Density for Actel 2 μm Technology FPGA Devices. This FPGA technology is several years old and the reliability data base on it is new and still evolving. See the manufacturer's reliability report and data sheets for details of the functional characteristics of this device. According to Actel information, the first production run of 1020B FPGA devices started in late 1989. For additional details, contact M. Davarpanah, JPL component specialist.

NOTE

The Actel data sheets for the ACT 1010/1020 FPGA chip refer to the fab-process description for this device as "2 μm". (See Data Sheet, Table 1).

However, JPL product analysis results of the FPGA device, with package markings A1020 and chip logo ACT1020B, reveal and identify the poly gate length of this chip to be approximately 1.4 μm and the effective channel length 1.24 μm, as shown in Figures 1a, 1f, 10c, and 10d.

These dimensional results show the poly gate and effective channel length fab-process more closely approximates 1.5 or 1.2 μm, rather than the 2 μm definition.

This dimensional description and issue for Actel FPGA devices 1020, 1020A, and 1020B needs to be specifically identified in Actel's data sheets for each device type, together with corresponding package/lid markings in terms of quality assurance specifying FPGA chip type in ceramic package.

Procedure:

This evaluation was performed on one device in accordance with MIL-STD 883C, Methods for Microcircuits.

The chip was extracted from its PGA package, backscribed and cleaved into four segments.

Two chip segments were used for lateral selective exposure and removal of chip materials levels. The other two chip segments were prepared as cross-section samples and examined for definition and identification of chip materials layers on Si, their interface integrity and thickness dimensions (see Table I). Optical and SEM examinations were performed prior to and after each level of chip materials exposure, and X-ray spectroscopic analysis was used for identification of chip materials composition.

Table I. Physical Dimensions of ACT 1020B Die and Die Structures

	Die/Die Structures	Dimensions
1	Die material: Si and size	≈ 8.8 x 9.2 μm
2	Die passivation: Nitride on SiO_2	≈ 1.2 μm
3	Die metallization: Si-and-cu doped Al two-level interconnect, metal-2 top and metal-1 bottom level	
4	Metal-2 thickness	≈ 1. μm
5	Metal-2 step thickness in vias	≈ 0.25 μm
6	Metal-2 line width	≈ 4. μm
7	Metal-1 thickness	≈ 0.85 μm
8	Metal-1 step thickness in BPSG apertures	≈ 0.2 μm
9	Intrametal dielectric SOG on LTO (not planarized) thickness	≈ 0.65 μm
10	BPSG thickness	≈ 0.75 μm
11	Thin nitride thickness on field oxide	≈ 800. Å
12	Field oxide thickness	≈ 0.75 μm
13	Gate poly thickness	≈ 0.35 μm
14	Poly gate length	≈ 1.45 μm
15	Effective chan-length	≈ 1.24 μm
16	Gate oxide thickness	≈ 250. Å
17	ONO thickness	≈ 1000. Å
18	PAL-poly thickness	≈ 0.35 μm
19	Contact dia to poly and Si	≈ 2. μm

NOTE: The chip materials dimensions were derived from SEM photo figures using the SEM calibration reference line and magnification factor.

OPTICAL PHOTO VIEWS OF ACTEL/MAT CMOS-PAL DEVICE IN PGA PACKAGE AND EXPOSED Si-CHIP IN PACKAGE CAVITY, AND CHIP CIRCUIT SEGMENTS (2 μm PROC).

Figure 1a. 1.5X view of PGA ceramic package with metal lid and markings.

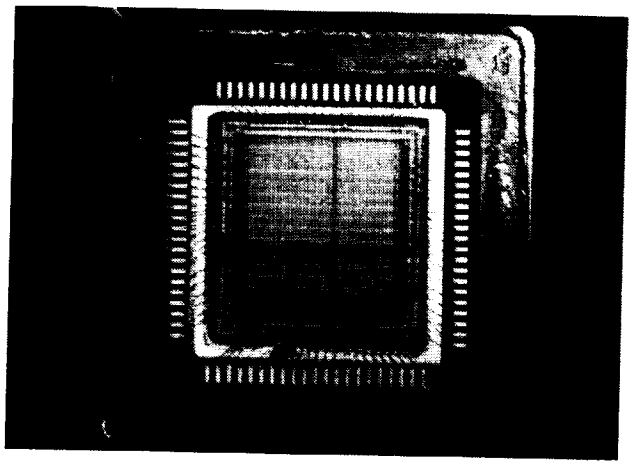


Figure 1b. 3.5X view of exposed package cavity with PAL chip and lead frame with wire bonds to chip pads.

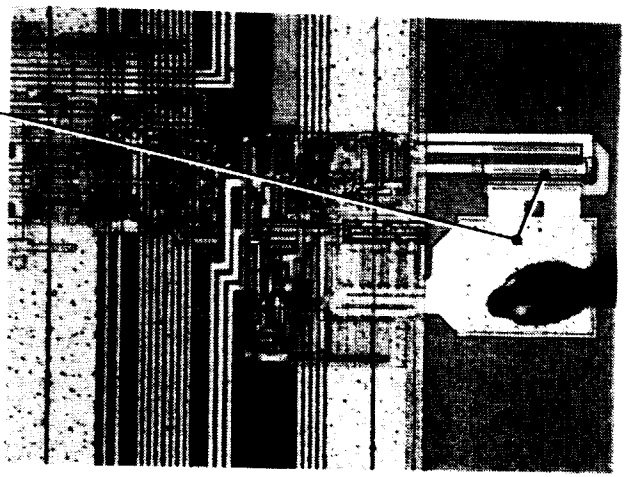


Figure 1c. 200X view of PAL chip circuit segment with 2-level metal interconnect and nitride passivation.

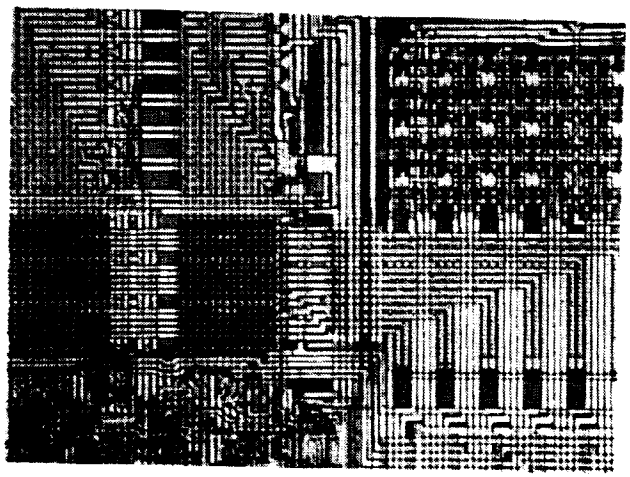


Figure 1d. 250X view of chip circuit segment with metal interconnections and nitride passivation.

SEM PHOTO VIEWS OF ACTEL-PAL CHIP CIRCUIT SEGMENTS.

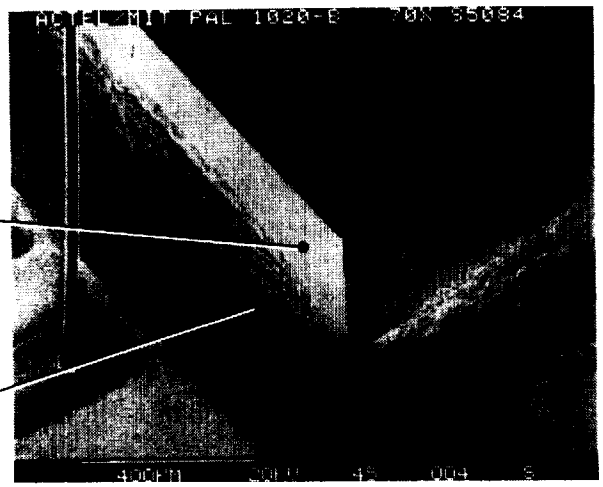


Figure 1e. 70X view of die corner dicing features and attach fillet.

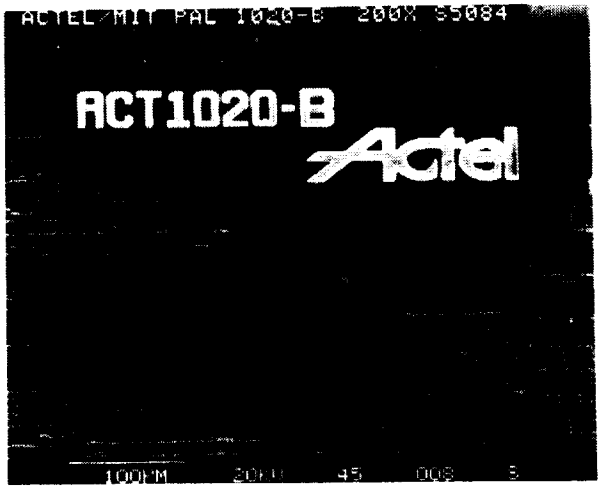


Figure 1f. 200X view of chip segment with logo.

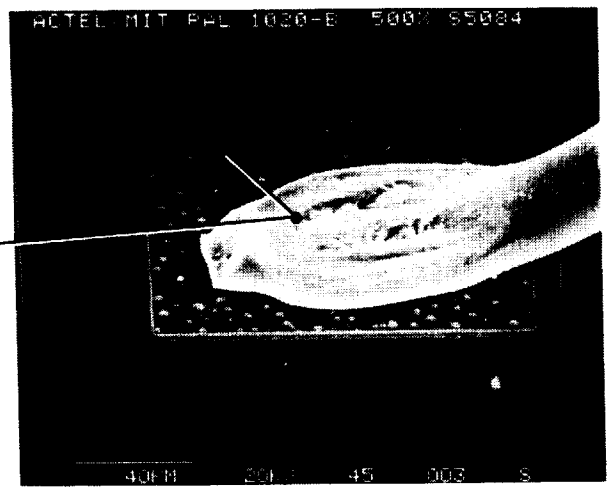


Figure 1g. 500X view of Al-wire bond compression features to die pad.

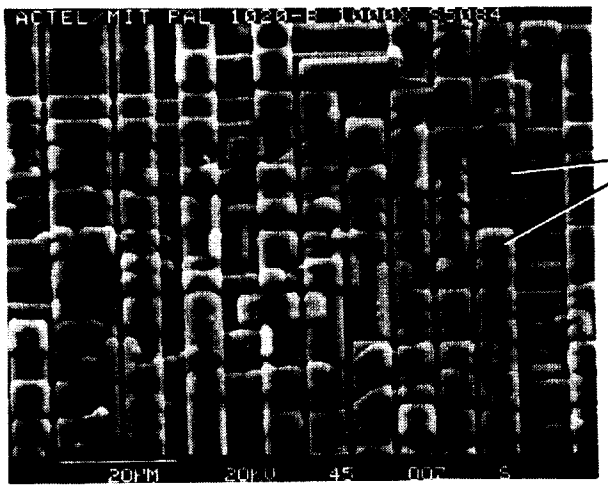


Figure 1h. 1kX view of nitride passivation morphology over chip metal interconnections.

SEM PHOTO VIEWS OF EXPOSED TOP LEVEL Al-METAL-2 INTERCONNECT WITH CONTACTS TO METAL-1 AND STEP COVERAGE FEATURES (TOP NITRIDE AND SiO_2 REMOVED).

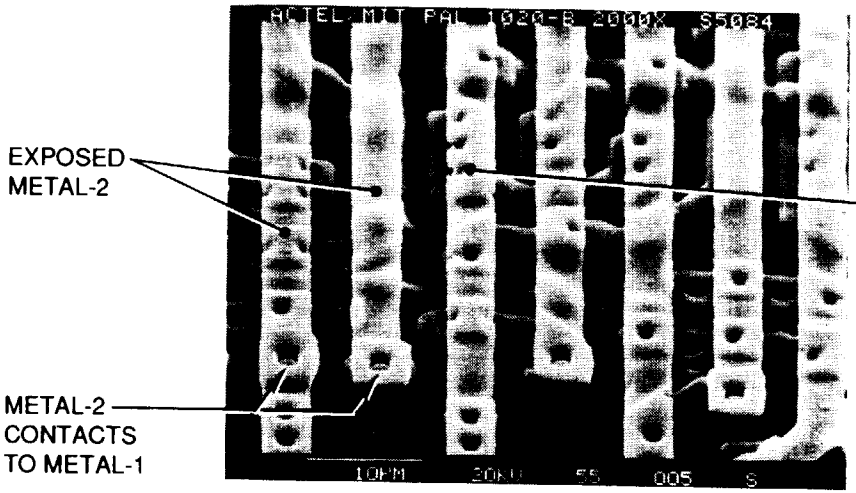


Figure 2a. 2kX view of exposed metal-2 line widths and contacts.

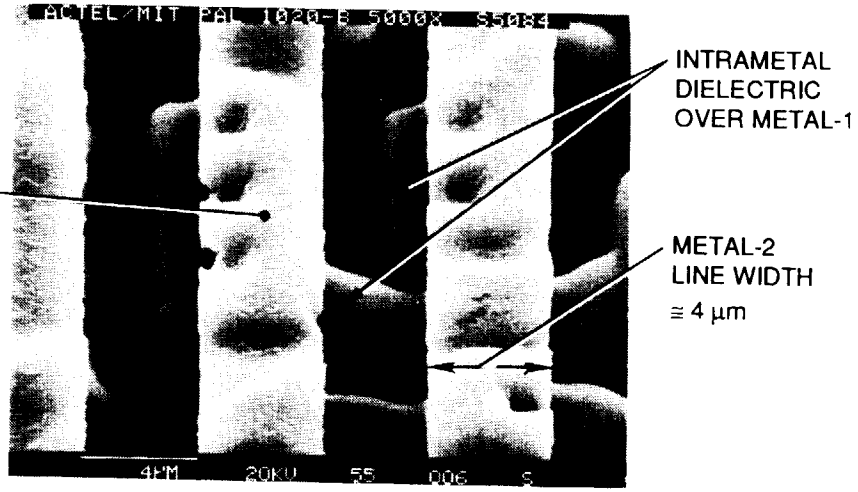


Figure 2b. 5kX view of metal-2 line width pattern.

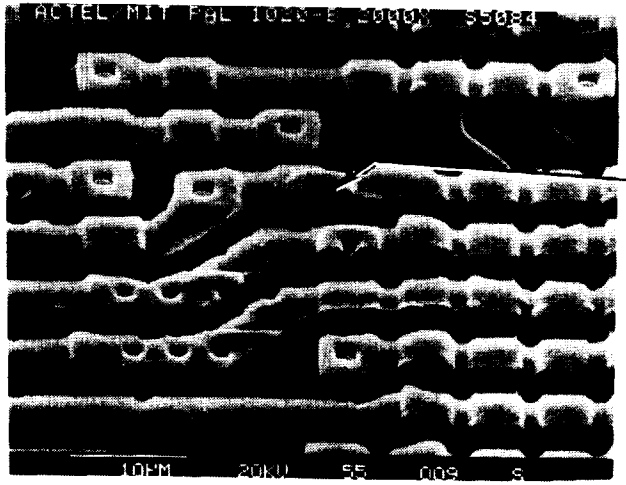


Figure 2c. 2kX side view of metal-2 step coverage and contacts to metal-1.

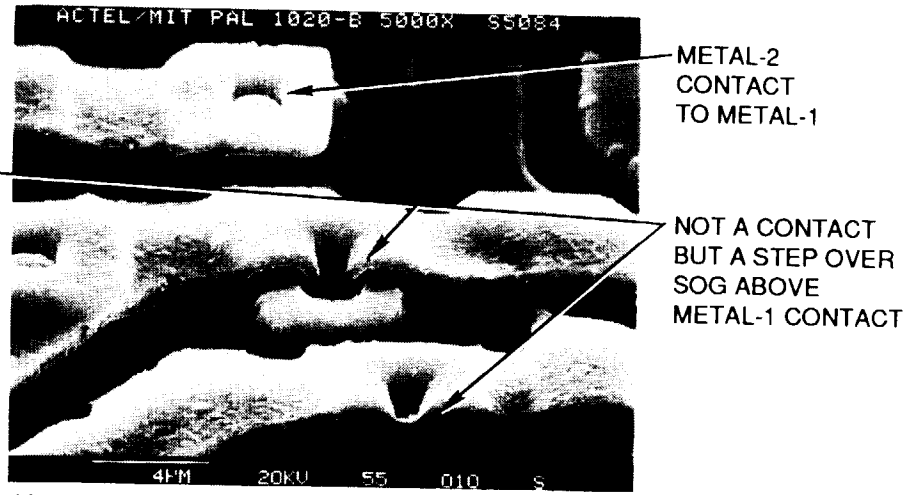


Figure 2d. 5kX side view of metal-2 step coverage features over SOG and contacts of metal-1.

SEM PHOTO VIEWS OF EXPOSED TOP LEVEL Al-METAL-2 INTERCONNECTIONS TO METAL-1 AND STEP COVERAGE FEATURES (TOP NITRIDE AND SiO_2 REMOVED).

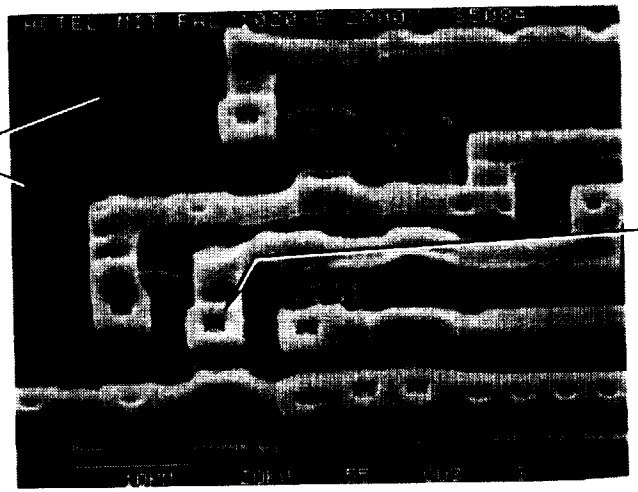


Figure 3a. 2kX side view of exposed metal-2 step features and contacts to metal-1.

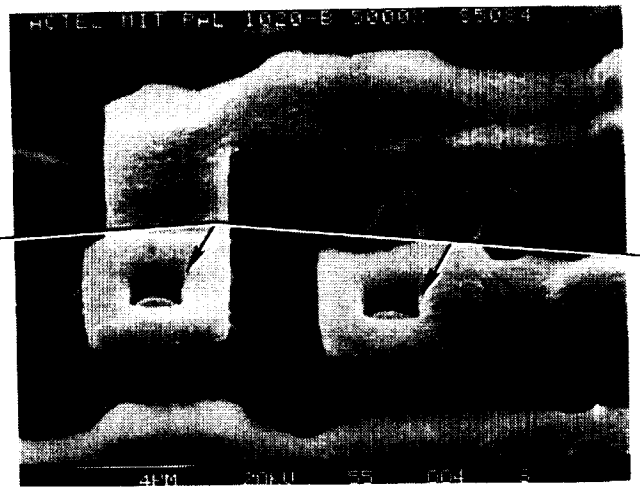


Figure 3b. 5kX side view of metal-2 contact features to metal-1.

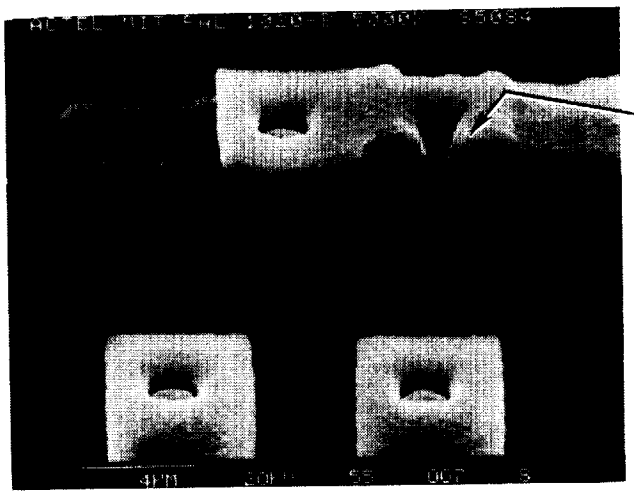


Figure 3c. 5kX view of metal-2 contacts to metal-1.

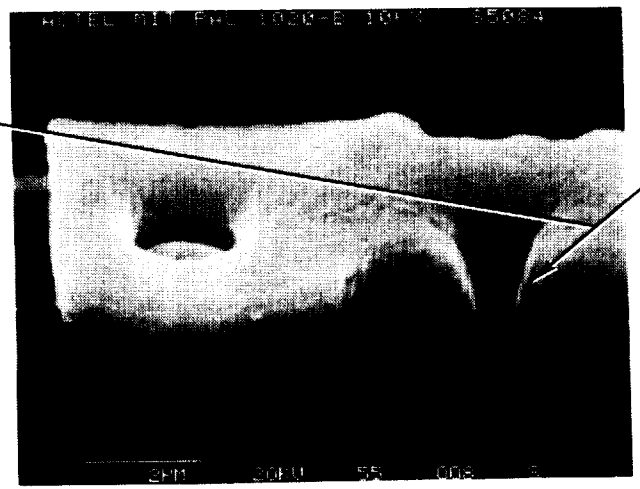


Figure 3d. 10kX side view of metal-2 contact to metal-1, and metal-2 step features over SOG and contact of metal-1.

SEM PHOTO VIEWS OF EXPOSED METAL-2 ONLY (TOP NITRIDE AND SiO_2 REMOVED).

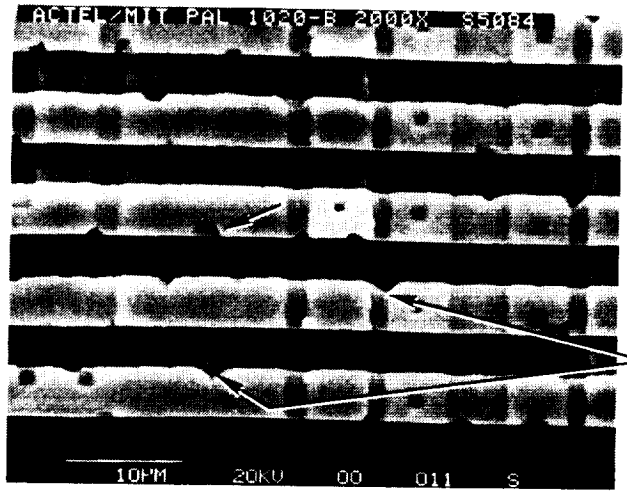


Figure 4a.
2kX flat view of metal-2 line widths with minor wedge defects in metal.

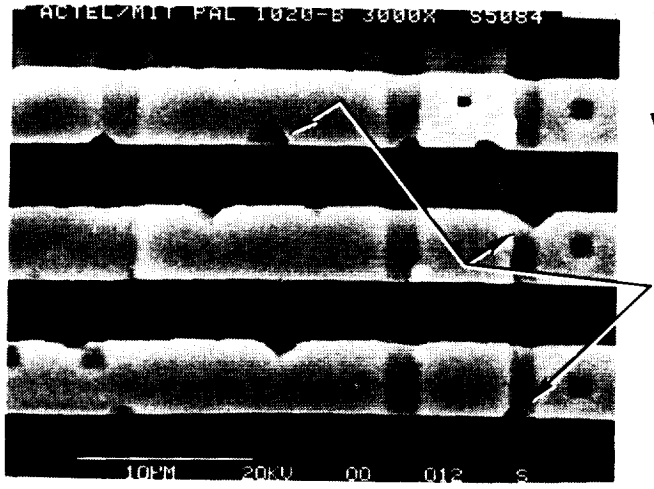


Figure 4b.
3kX flat view of metal-2 line width with minor wedge defects.

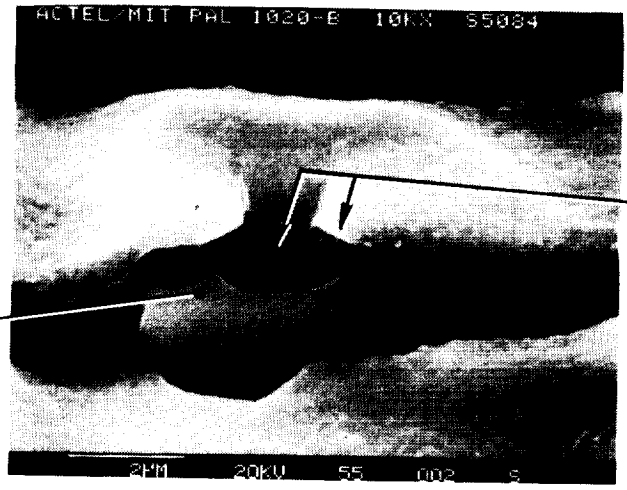


Figure 4c.
10kX side view of metal-2 step over SOG and SiO_2 step of metal-1 contact.

SEM PHOTO VIEWS OF EXPOSED METAL-2 AND METAL-1 (INTRAMETAL DIELECTRICS REMOVED).

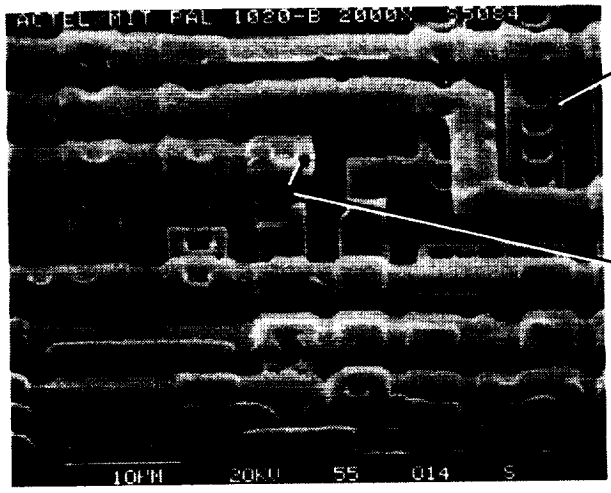


Figure 5a. 2kX side view of metal-2 step coverage and contacts to metal-1.

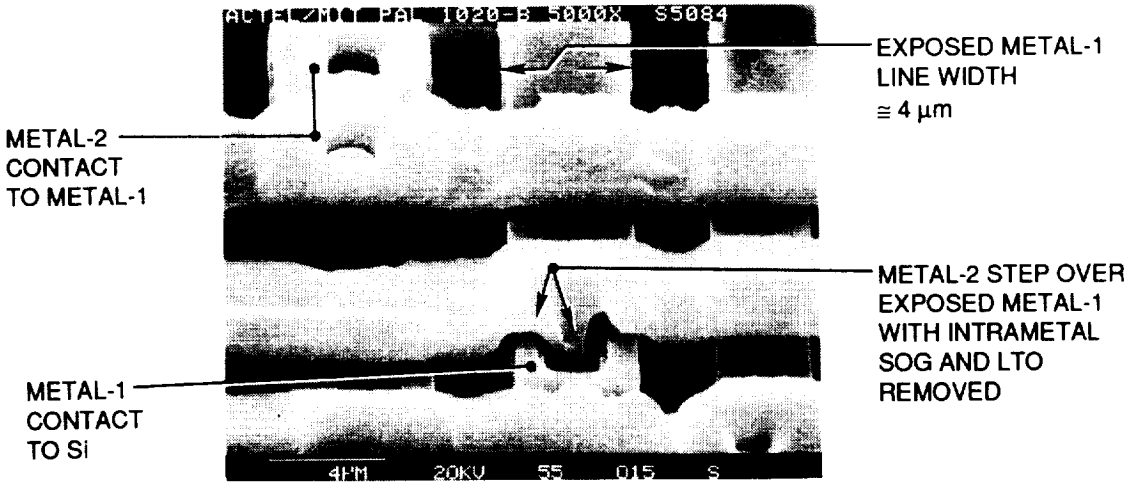


Figure 5b. 5kX side view of metal-2 step coverage features and contact to metal-1.

SEM PHOTO VIEWS OF EXPOSED METAL-2 AND METAL-2 INTERCONNECTIONS (INTRAMETAL DIELECTRICS REMOVED).

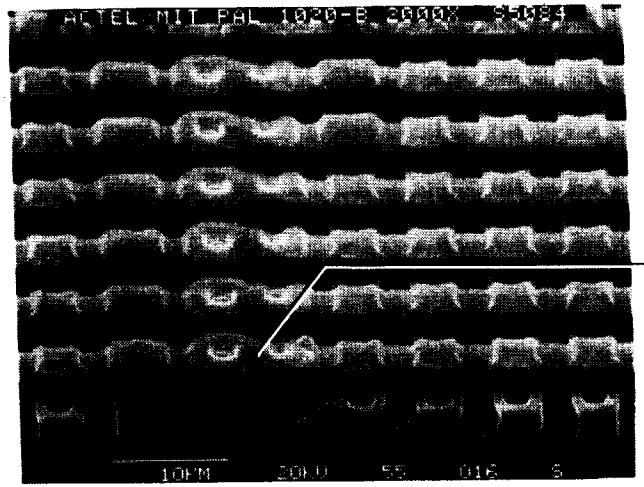


Figure 6a. 2kX side view of PAL array circuit segment exposed metal-2 and metal-1 interconnections.

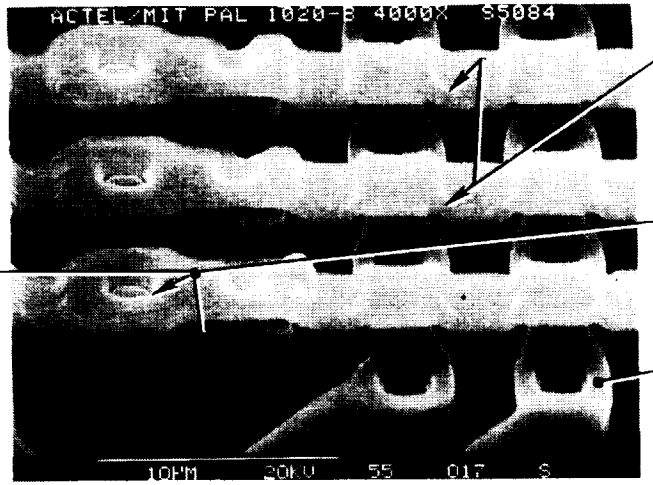


Figure 6b. 4kX side view of metal-2 contacts to metal-1 and metal-1 to Si.

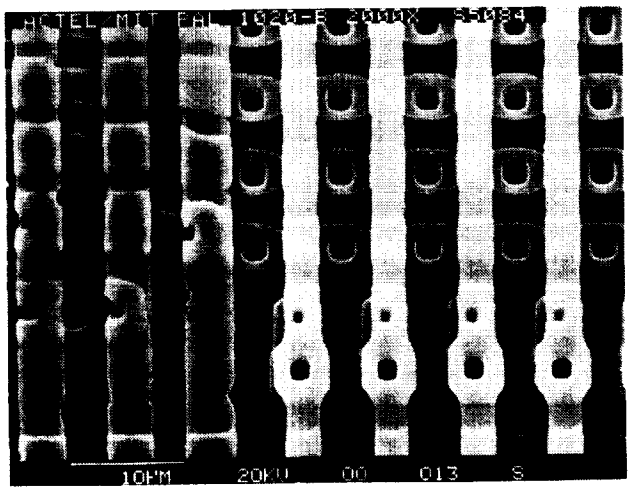


Figure 6c. 2kX flat view of PAL array circuit segment exposed metal-2 and metal-1 contact patterns.

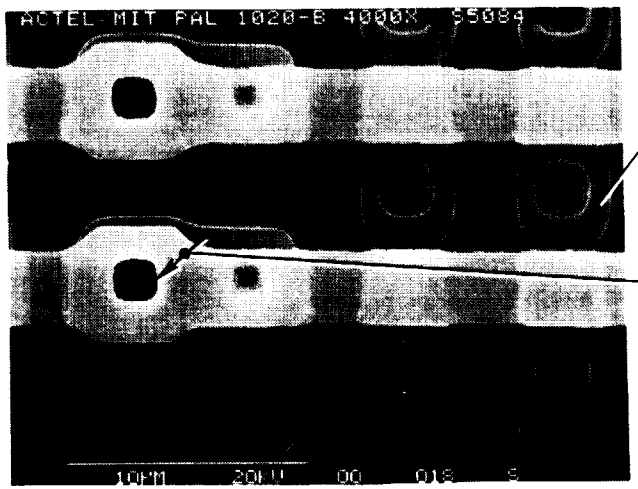


Figure 6d. 4kX flat view of metal-2 contacts to metal-1 and metal-1 contacts to Si.

SEM PHOTO VIEWS OF EXPOSED CONTACTS TO POLY AND SI, AND THIN NITRIDE FILM OVER POLY PATTERNS AND FIELD OXIDE (TWO LEVEL METAL INTERCONNECT AND BPSG REMOVED).

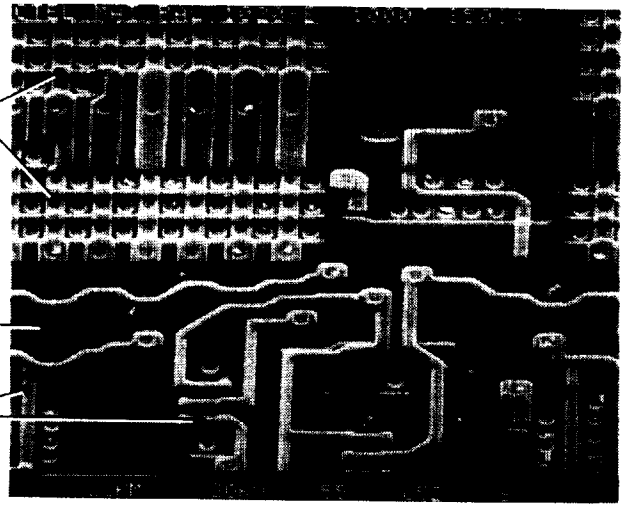


Figure 7a. 1kX side view of PAL circuit segment, and gate patterns.

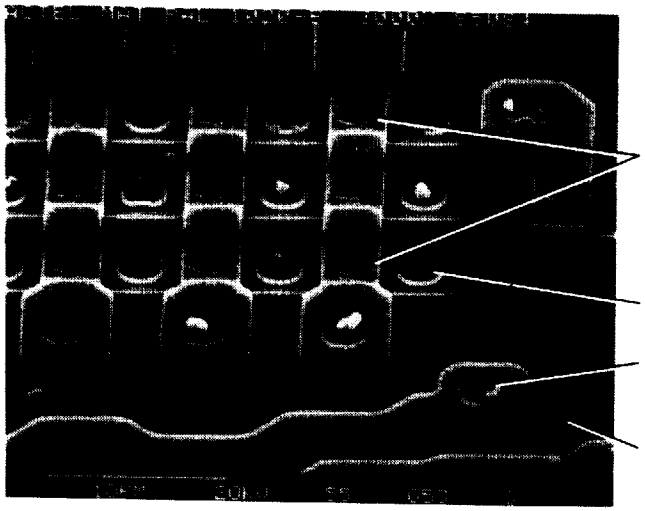


Figure 7b. 3kX side view of PAL circuit segment with poly pattern programmed contact to Si.

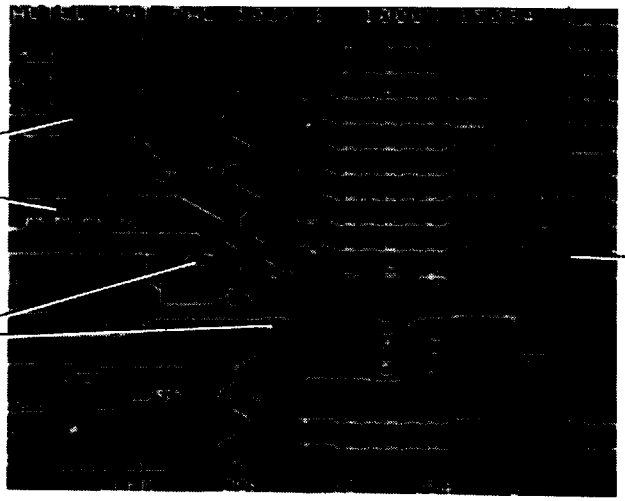


Figure 7c. 1000X side view of PAL circuit segment poly, and transistor gates.

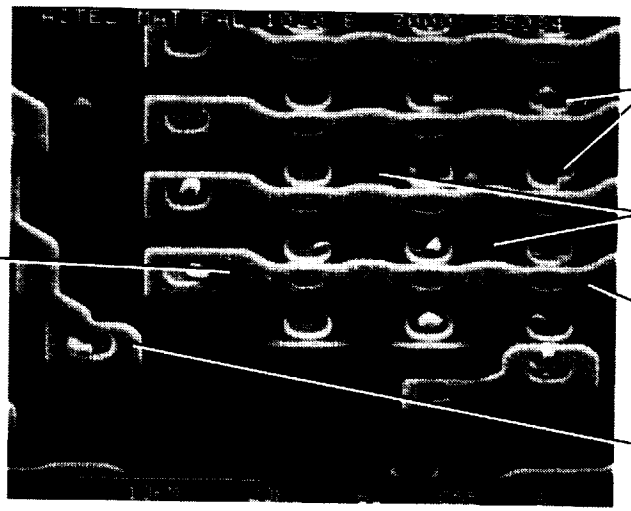


Figure 7d. 3kX view of programmable array logic segment poly pattern with fused contacts to Si.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE PATTERNS ON SILICON SUBSTRATE.

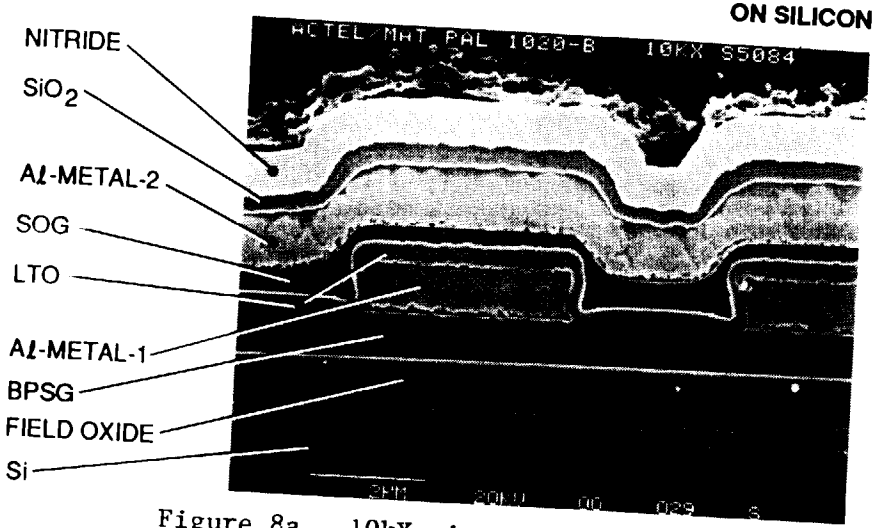


Figure 8a. 10kX view insulating dielectric levels and two-level Al-metal (metal-2 top, metal-1 bottom).

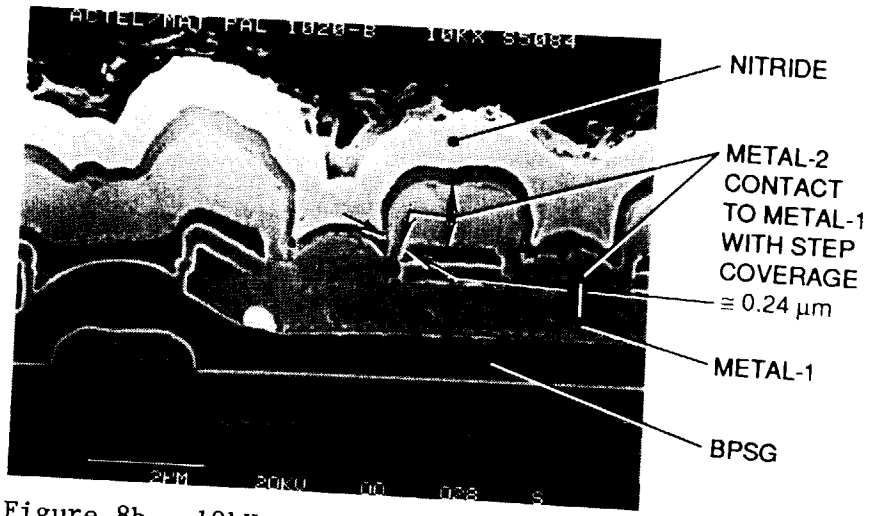


Figure 8b. 10kX view of metal-2 contacts to metal-1 and step coverage features.

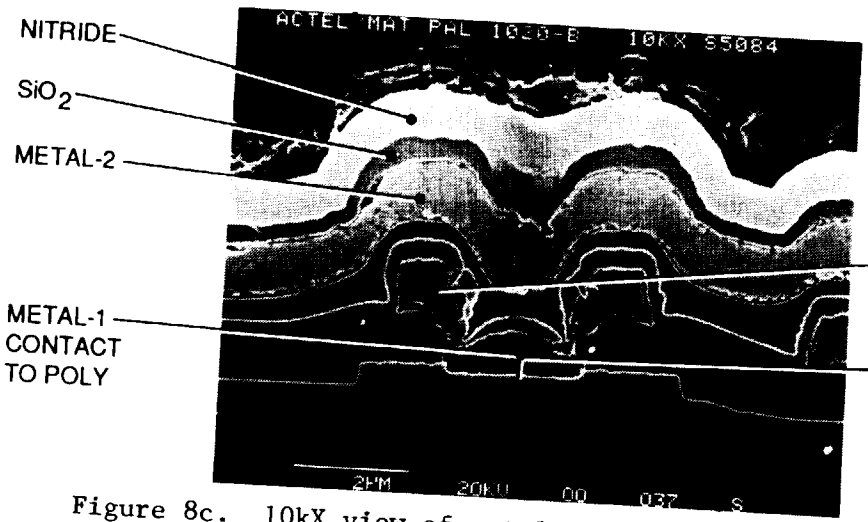


Figure 8c. 10kX view of metal-1 contact to poly pad on thick field oxide and metal-1 step coverage in BPSG via cut.

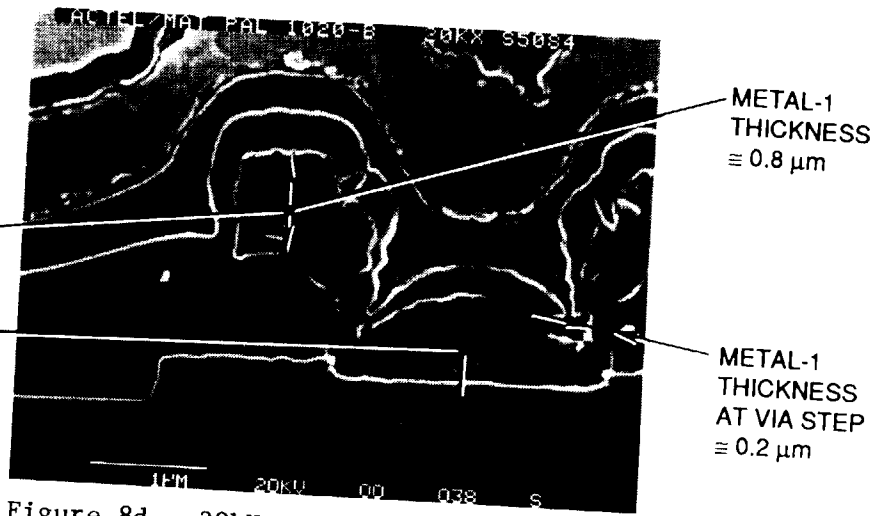


Figure 8d. 20kX view of metal-1 contact to poly and metal step coverage thickness in BPSG via cut.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE PATTERNS ON Si SUBSTRATE.

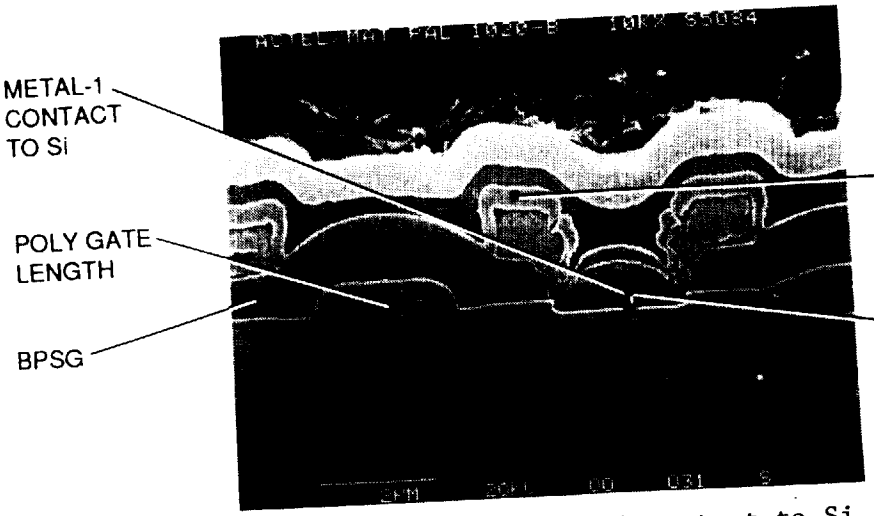


Figure 9a. 10kX view of metal-1 contact to Si, and poly gate length pattern on gate oxide.

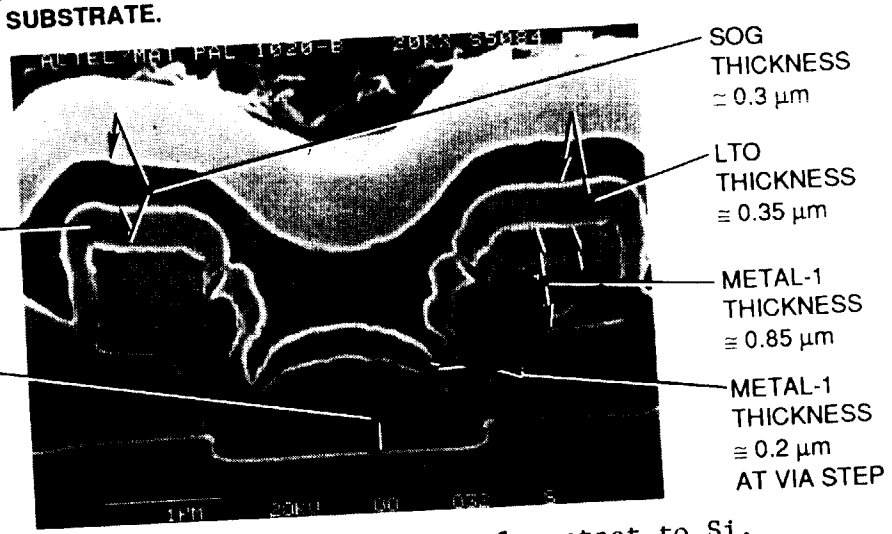


Figure 9b. 20kX view of metal contact to Si, and metal step coverage thickness in BPSG via sidewall cut.

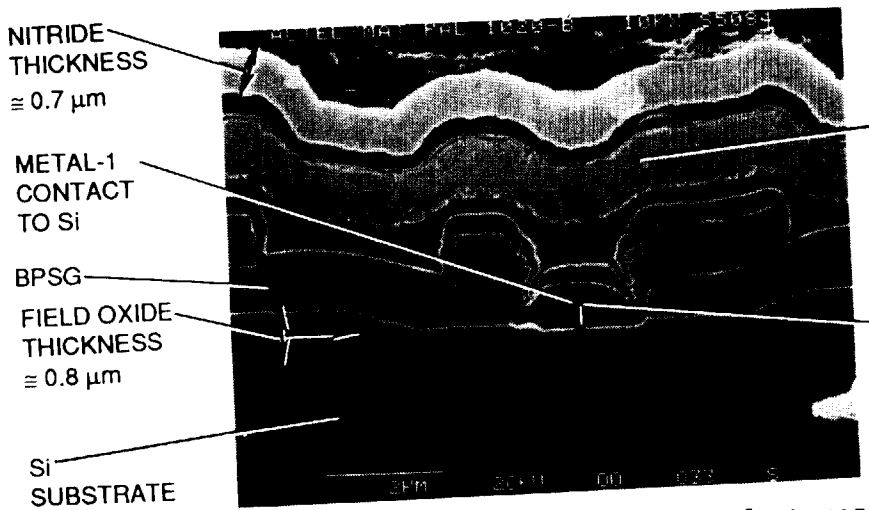


Figure 9c. 10kX view of metal-1 contact features to Si and step coverage.

Figure 9d. 20kX view of metal-1 contact to Si and metal-1 step thickness at BPSG via sidewall cut.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE ON Si SUBSTRATE.

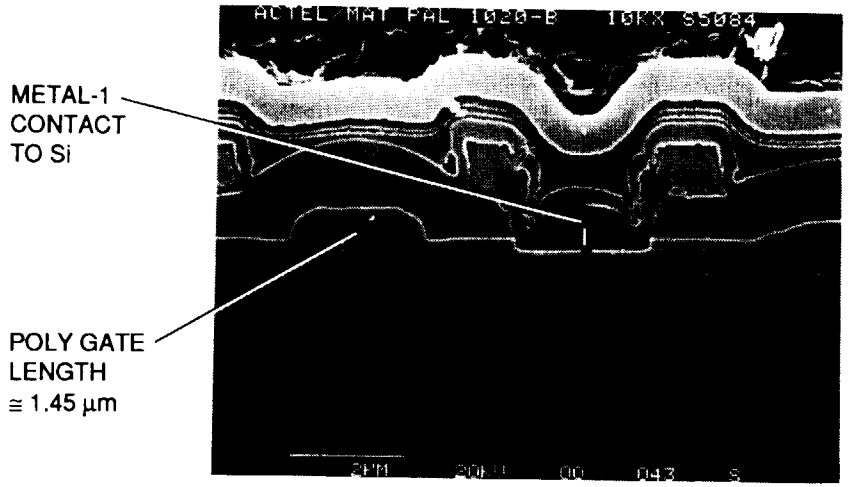


Figure 10a. 10kX view of metal-1 contact features to Si, and poly gate channel length on thin gate oxide.

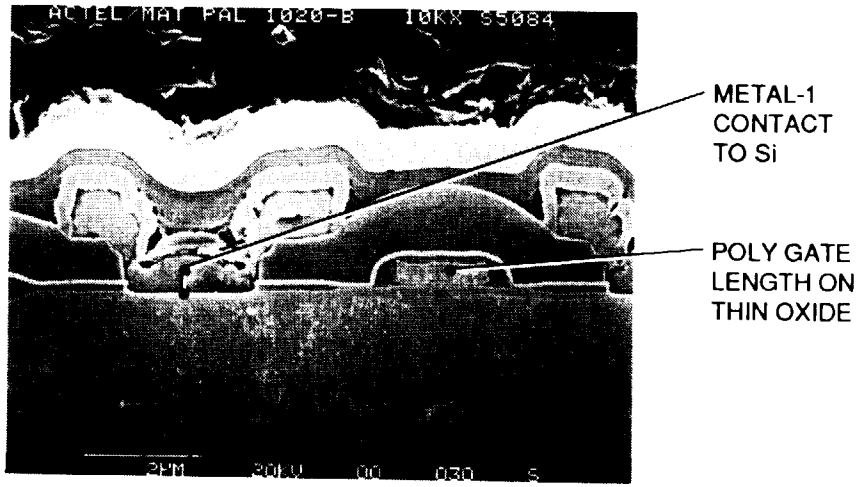


Figure 10b. 10kX view of another metal-1 contact features to Si, and poly gate length pattern on thin gate oxide.

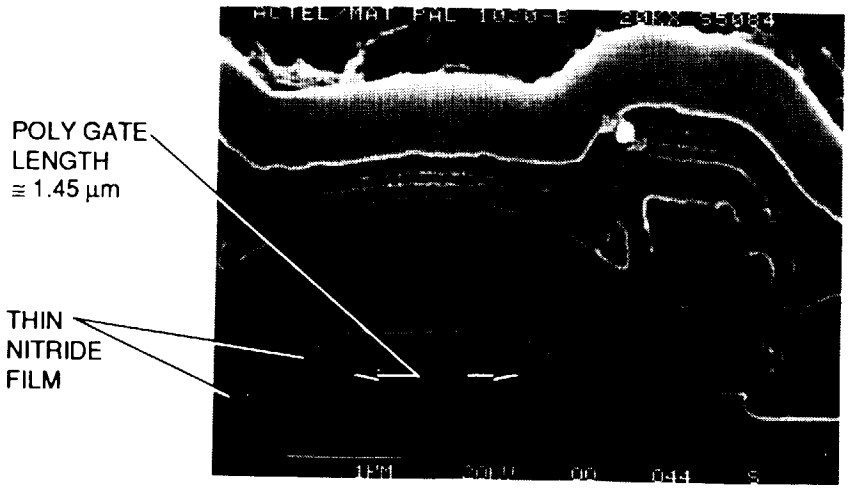


Figure 10c. 20kX view of poly gate length on thin gate oxide.

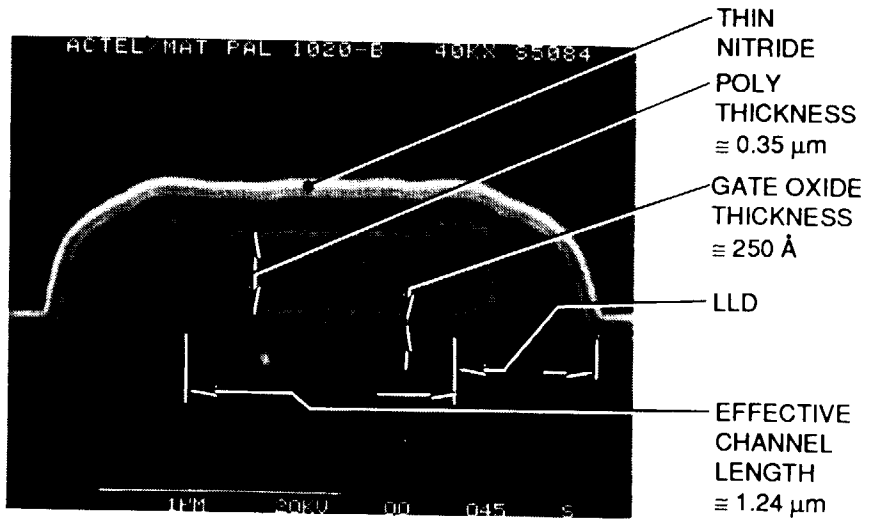


Figure 10d. 40kX view of poly gate thickness, poly gate length, and effective chan length, and gate oxide thickness.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED PATTERNS OF PROGRAMMABLE POLY (ANTIFUSE) ON (ONO – OXIDE-NITRIDE-OXIDE) PAL LOGIC STRUCTURE ON N^+ Si; PROGRAMMED – POLY FUSED WITH Si (AS IN BURIED CONTACT) AND UNPROGRAMMED WITH ONO BETWEEN POLY AND Si.

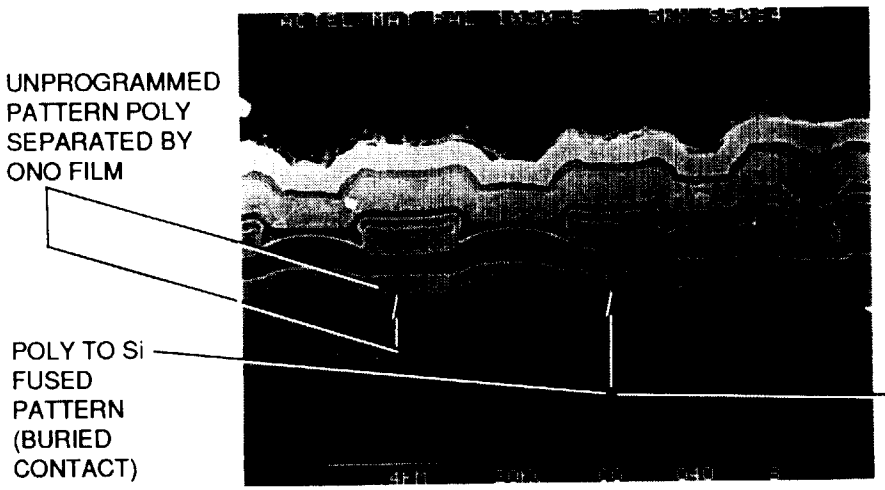


Figure 11a. 5kX view of poly programmable link segment on ONO unprogrammed, and programmed (fused) pattern to Si.

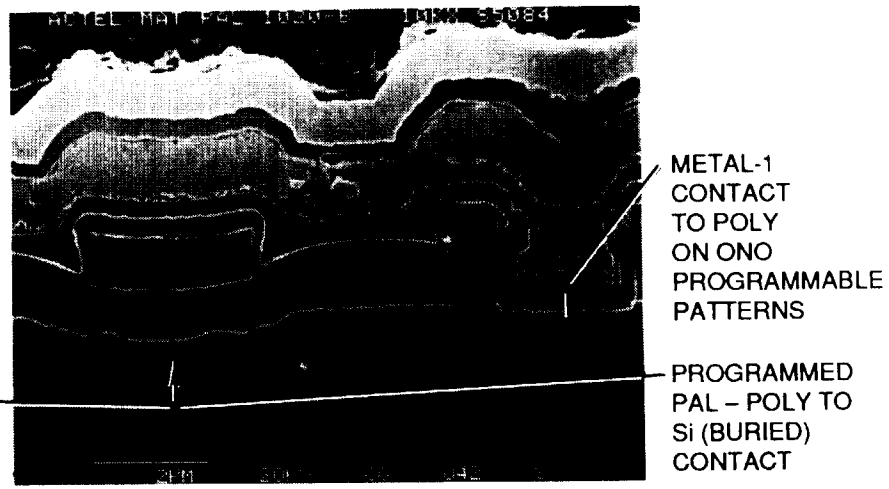


Figure 11b. 10kX view of PAL poly with programmed contact to Si through ONO film.

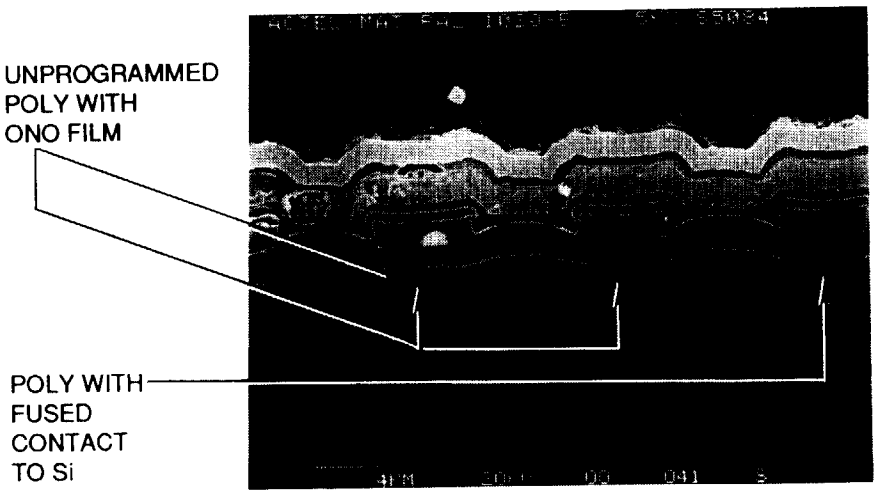


Figure 11c. 5kX view of PAL-poly programmed and unprogrammed patterns.

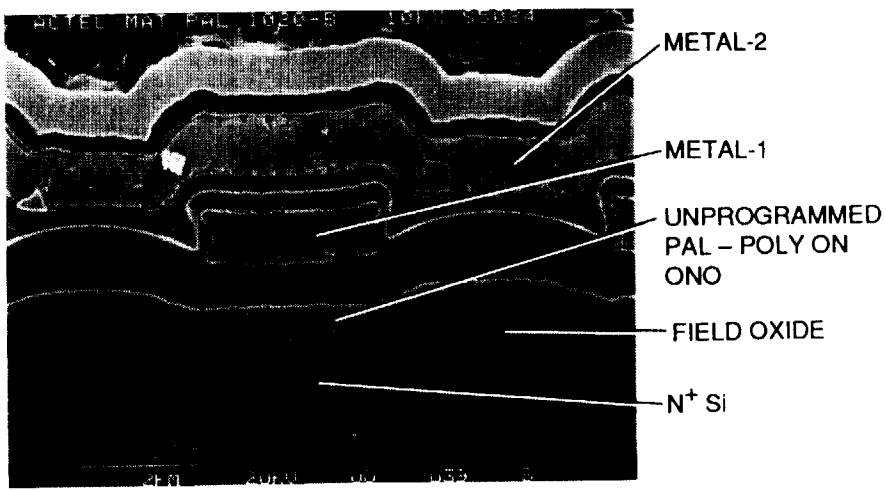


Figure 11d. 10kX view of PAL-poly unprogrammed pattern with intact ONO between poly and Si.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED PATTERNS OF PROGRAMMABLE POLY (ANTIFUSE) ON (ONO – OXIDE-NITRIDE-OXIDE) PAL LOGIC STRUCTURE ON N^+ Si; PROGRAMMED POLY FUSED WITH Si AS IN BURIED CONTACT, AND UNPROGRAMMED WITH ONO BETWEEN POLY AND Si (FIG. 11a-11d).

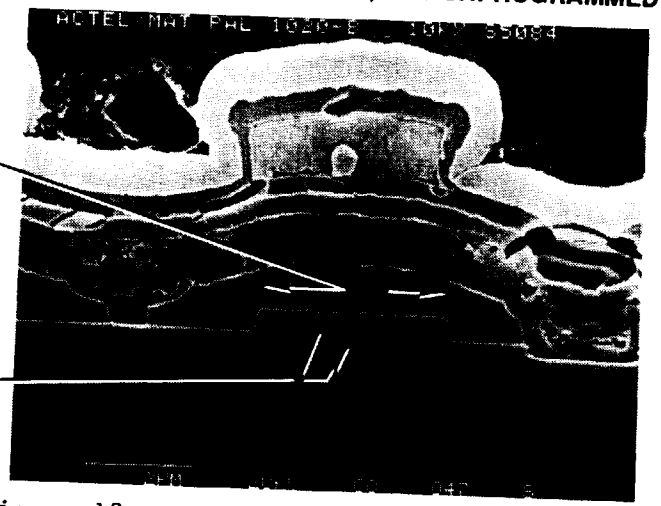


Figure 12a. 10kX view of PAL-poly on ONO unprogrammed pattern.

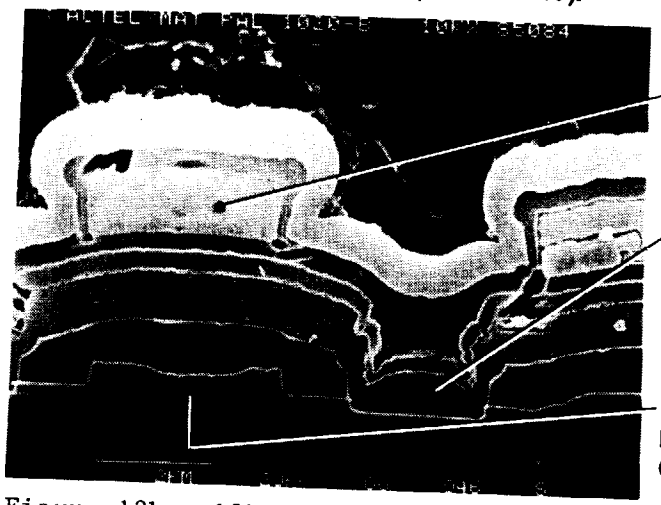


Figure 12b. 10kX view of PAL-poly programmed pattern (fused) to Si, and metal-1 contact to N^+ Si.

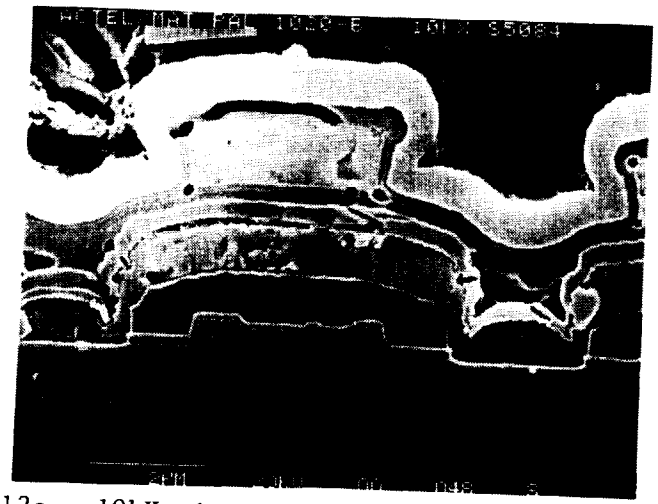


Figure 12c. 10kX view of another PAL-poly with fused (buried) contact to Si, and metal-1 contact to Si.

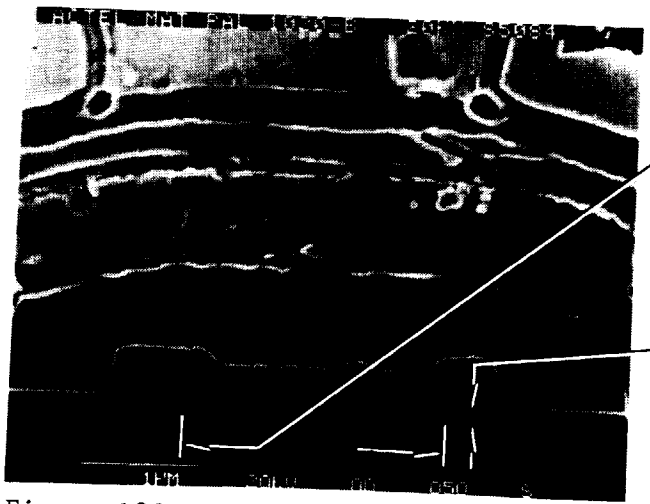


Figure 12d. 20kX view of PAL-poly fused (buried) contact features with Si (N^+).

ACT™ 1010/1020 Reliability Report

By Steve Chiang and Ken Hayes

ACT™ 1010/1020 devices are 1200- and 2000-gate (respectively) field programmable gate arrays (FPGAs). The programming element is an Actel-invented PLICE™ (Programmable Low-Impedance Circuit Element) antifuse. An antifuse is a normally open device in which an electrical connection is established by the application of a programming voltage. Although ACT 1010/1020 products are one-time programmable devices, their unique architecture features complete functional testability.

The ACT 1010/1020 device is processed using a standard 2 µm, double metal, CMOS process to which three additional masking steps have been added to implement the PLICE antifuse. A description of the main process parameters is shown in Table 1. Because ACT 1010/1020 devices are manufactured with a conventional CMOS process, normal CMOS failure modes will be observed. However, the addition of the antifuse adds another structure that could affect the device's reliability.

Actel has completed numerous studies in order to quantify the reliability of the antifuse. These studies lead to the conclusion that the time to failure of the antifuse is substantially more than 40 years under normal operating conditions and that the combined contribution of all antifuses to the gate array product's hard failure rate is less than 10 FITS (Failures-in-Time or 0.001% failures per 1000 hours).

Table 1. ACT 1010/1020 Process Description

CMOS, 2 µm, double metal, dual polysilicon, dual well, EPI wafer.

Dimensions	Width	Space
N+	4.0 µm	2.0 µm
P+	4.0	2.0
Cell Polysilicon	1.6	3.6
Gate Polysilicon	1.6	2.4
Metal I	4.0	2.0
Metal II	4.2	2.8
Contact	1.8 x 1.8	2.0
Via	2.0 x 2.0	2.0

Thickness	
Normal Gate Oxide	25 nm
High Voltage Gate Oxide	40
Cell Polysilicon	35
Gate Polysilicon	40
Metal I	80
Metal II	100
Passivation	1100

Composition	
Metal I	98% Al, 1% Si, 1% Cu
Metal II	98% Al, 1% Si, 1% Cu
Passivation	300 nm SiO_2, 800 nm SiN

PLICE Antifuse Reliability

The antifuse is a vertical, two-terminal structure. It consists of a polysilicon layer on top, N+ doped silicon on the bottom, and an ONO (oxide-nitride-oxide) dielectric layer in-between. A Scanning Electron Microscope (SEM) cross-section of the antifuse is shown in Figure 1. On the ACT 1010/1020 device, the size of the antifuse is 1.8 μm^2. This small size, along with a low programmed on-resistance, typically 500 Ω, makes the PLICE antifuse a very attractive alternative to EPROM, EEPROM, or RAM for use as a programming element in a large programmable gate array. In the unprogrammed state, the resistance of the antifuse is in excess of 100 MΩ. The ACT 1010 and ACT 1020 contain 112,000 and 186,000 antifuses respectively. However, typical applications utilizing 85% of the available gates require programming only 2% to 3% of the available antifuses.

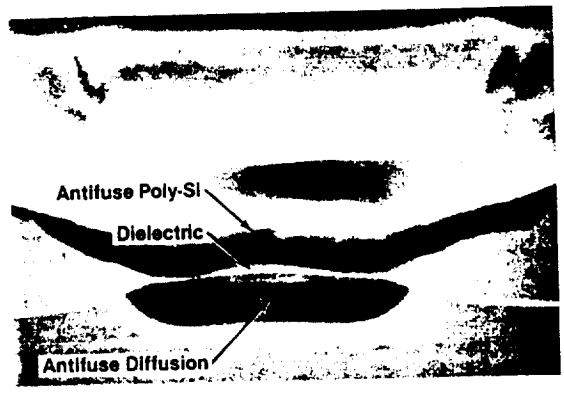


Figure 1. SEM Cross-Section of Antifuse

The Unprogrammed Antifuse

In order to evaluate antifuse reliability, Actel has developed models and collected data for both unprogrammed and programmed antifuses[1, 2]. We'll consider the unprogrammed antifuse first. Since the antifuse is a dielectric sandwiched between polysilicon and silicon, the model for its reliability, in the unprogrammed condition, is the same as that used to evaluate reliability of MOS transistor gate oxides. The parameter we wish to evaluate is the time to breakdown (t_{bd}) of the dielectric. This parameter is a function of the electric field across the dielectric as well as temperature and has the following relationship[3]

$$t_{bd} = t_0 \cdot \exp(G/E) \quad (1)$$

where t_{bd} is the time to breakdown in seconds, t_0 is a constant, E is the electric field in MV/cm, and G is the field acceleration factor in MV/cm (G is a function of temperature).

By taking the log of both sides of equation 1 we have:

$$\ln(t_{bd}) = G \cdot (1/E) + \ln(t_0) \quad (2)$$

From experimental data, we can plot the log of the time to breakdown of the antifuse at various temperatures versus the reciprocal of the electric field across it and derive G from the slope and t_0 from the Y axis intercept. Actel has done this both on large antifuse capacitors and on arrays of 28,000 antifuses. An example is shown in Figure 2. From this we have derived a value for G of 510 MV/cm and a t_0 of 1×10^{-16} seconds. Also note the difference between the data at 25°C and 150°C.

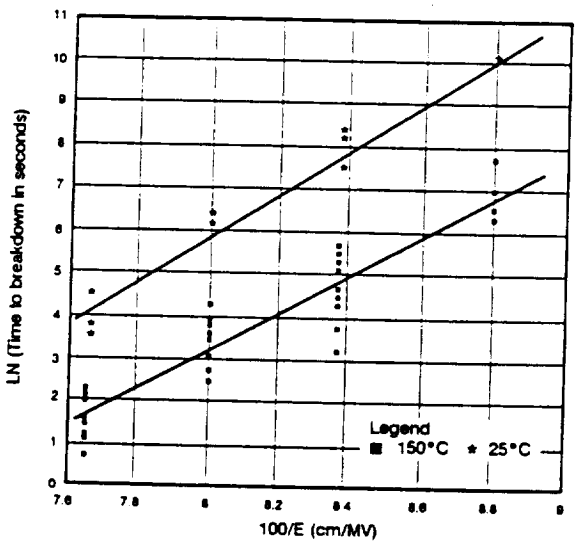


Figure 2. Field Acceleration of Antifuse (0.04 mm² Area Capacitor)

In order to quantify the temperature-dependence of the time to breakdown, we use the Arrhenius equation to determine the reaction rate (or semiconductor failure rate) of a given process (failure mode) over temperature:

$$R = R_0 \cdot \exp^{(-E_a/kT)} \quad (3)$$

where R is the reaction rate, R_0 is a constant for a particular process, T is the absolute temperature in degrees Kelvin, k is Boltzmann's constant (8.62×10^{-5} eV/°K), and E_a is the activation energy for the process in electron volts. To determine the acceleration factor for a given failure mode at temperature T_2 as compared with temperature T_1 we use equation 3 to derive:

$$A(T_1, T_2) = \exp[-(E_a/k) \cdot \{(1/T_1) - (1/T_2)\}] \quad (4)$$

where A is the acceleration factor.

For a given time to breakdown of a dielectric, the expression,

$$E_a = k \cdot d\ln(t_{bd})/d(1/T) \quad (5)$$

gives us the activation energy[2]. The field acceleration factor, G, is also temperature-dependent, i.e.

$$G(T) = G \cdot [1 + \delta/k \cdot \{1/T - 1/298\}] \quad (6)$$

where δ (in eV) characterizes the temperature-dependence of G.

E_a can be related to G (T) by:

$$E_a = G \cdot \delta/E - E_b \quad (7)$$

where δ and E_b are treated as fitting parameters between E_a and G.

From the data shown in Figure 2, as well as data on test arrays of 28,000 antifuses, we have derived a value for E_a of 0.2 eV. This value of E_a = 0.2 eV is for a very high E field of 11 MV/cm, or 10 V across the antifuse. With 5.5 V, the E field is about 6 MV/cm and E_a is approximately 0.6 eV. Values of δ and E_b were found from equation 7 to be 0.01 eV and 0.24 eV, respectively.

By combining equations 1, 5, 6, and 7, we obtain an overall equation for the time to breakdown for a given temperature and E field:

$$t_{bd} = t_0 \cdot \exp\{(G/E)[1 + (\delta/k) \cdot (1/T - 1/298)] - (E_b/k) \cdot (1/T - 1/298)\} \quad (8)$$

By applying the values for the constants as defined above, the time to breakdown for the antifuse dielectric can be derived for a given temperature and electric field. In Table 2, we have used equation 8 to solve for the acceleration factors associated with powering up a device at high voltage and/or temperature and comparing the failure rate with more typical voltages or temperatures. We can see the effect of temperature by comparing 125°C at 5.5 V with 55°C at 5.5 V in which the Actel model (equation 8) gives us an acceleration factor of 36, or 4.1 equivalent years for a 1000-hour burn-in at 125°C. Note that this acceleration factor of 36 is close to the value of 41.8 derived from the Arrhenius equation (equation 4) using an activation energy of 0.6 eV and the same temperatures. We use 0.6 eV as a general semiconductor failure mode activation energy when calculating failure rates from high-temperature operating life (HTOL) later in this report.

Table 2. Acceleration Factor vs. Operating Conditions (Unprogrammed Antifuse)

$t_0 = 1 \times 10^{-13}$ sec, G = 510 MV/cm, δ = 0.01 eV

Model	Temperature/Voltage		Acceleration Factor	Equivalent Years for 1000-Hour 125°C Burn-In
	High	Typical		
Fixed Voltage	125°C/5.5 V	55°C/5.5 V	36.0	4.1
	125°C/5.5 V	95°C/5.5 V	3.9	0.4
Fixed Temperature	25°C/5.5 V	25°C/5.25 V	48.7	5.6
	25°C/5.75 V	25°C/5.25 V	1692	193.2
	25°C/5.75 V	25°C/5.5 V	34.7	4.0
Varied Temperature and Voltage	125°C/5.5 V	55°C/5.25 V	1526	174.2
	125°C/5.75 V	55°C/5.5 V	883	100.8
	125°C/5.75 V	95°C/5.5 V	96.5	11.0
Fixed 0.6 eV (Activation Energy), Voltage-Independent	125°C/5.5 V	55°C/5.5 V	41.8	4.8
	125°C/5.5 V	95°C/5.5 V	4.2	0.5

We can also see from Table 2 that a small change in voltage is a much more effective reliability screen for the unprogrammed antifuse than is a change in temperature. For example, if we compare 25°C at 5.75 V to 25°C at 5.25 V we see that just a half volt change yields an acceleration factor of 1692, or 193.2 equivalent years per 1000 hours at 5.75 V. This strong dependence on voltage allows Actel to screen out antifuse infant mortality failures during normal wafer sort testing at Actel simply by performing a special test in which a higher than normal voltage is applied across all antifuses. Because antifuse infant mortality failures can be detected and effectively screened, ACT 1010/1020 devices have as high a level of reliability as standard CMOS processed products.

Actel has collected data on over 350 antifuse test devices representing eleven wafer runs. From this data, we have determined that the contribution of the antifuse to overall device reliability is less than 10 FITS. This conclusion is confirmed by the reliability data taken on actual ACT 1010/1020 units which will be discussed later in this paper.

The Programmed Antifuse

A Kelvin test structure as shown in Figure 3 was used to evaluate reliability of a programmed antifuse. Here, a strip of polysilicon crosses an N+ diffusion. The antifuse is located at their intersection. There are metal-to-poly contacts at nodes 1 and 3 as well as metal-to-N+ contacts at nodes 2 and 4. A four-terminal Kelvin structure is useful should a failure occur, because antifuse opens can be separated from other problems (such as polysilicon or contact opens) simply by checking for continuity on appropriate pairs of nodes.

Test devices were stressed by forcing a constant 5 mA current from polysilicon to N+ diffusion through the antifuse at 250°C. Note that this stress is far greater than what a programmed antifuse would see in a device operating under normal conditions. Because the antifuse is used to connect two networks together, there is usually no voltage across it, hence no current passes through. A voltage will appear across the antifuse only momentarily while a network switches from low-to-high or high-to-low.

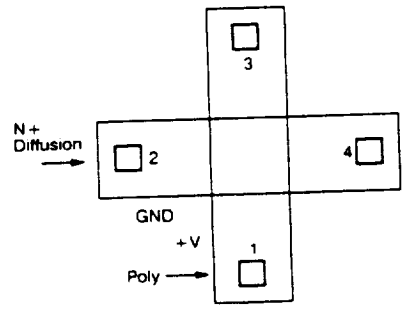


Figure 3. Antifuse Kelvin Structure

During the 5 mA, 250°C stress, the voltage across the antifuse was monitored. Figure 4 is a plot of the monitored voltage as a function of stress time. A sudden increase in voltage indicates that an open occurred. As can be seen from the figure, failures occurred at about 300 hours of stress. However, by probing on nodes 3 and 4 of the Kelvin structure, we were able to measure continuity and determine that the cause of failure was not the antifuse. The failed units were then examined on an SEM, where the cause of failure was revealed as metal-to-poly contact electromigration. This is a well-known failure mode in CMOS, which has been determined to have an activation energy of 0.9 eV. Using equation 4 we can predict a lifetime under normal operating conditions in excess of 40 years for this failure mode. The lifetime of the programmed antifuse is even longer.

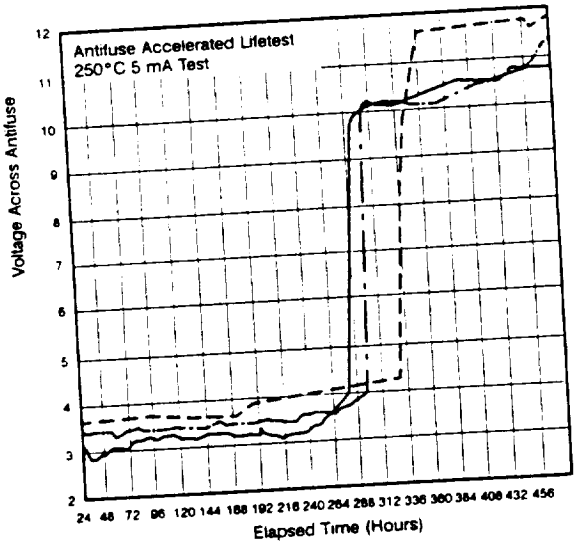


Figure 4. Voltage Across Antifuse versus Stress Time

ACT 1010/1020 Device Reliability

Device reliability was evaluated on four Actel products: a 64K PROM (PROM64), a 300-gate FPGA (1003), a 1200-gate FPGA (ACT 1010/1010A), and a 2000-gate FPGA (ACT 1020/1020A). The PROM64 product uses the same process and antifuse as the ACT 1010/1020. The 1003 is a test device, a smaller version of the ACT 1010/1020, which was used for early characterization and qualification. The ACT 1010A and ACT 1020A are 20% linear die shrink versions of the ACT 1010 and ACT 1020, respectively. The PROM64 units were packaged in 24-pin side-brazed packages; the FPGA units were in 68- and 84-pin JLCC (ceramic J-leaded chip carriers) and PLCC (plastic-leaded chip carriers) packages. Package characteristics for ACT 1010/1020 devices are shown in Table 3.

Table 3. ACT 1010/1020 Package Characteristics

PLCC	
Molding Compound	Sumitomo 6300 H
Filler Material	Fused silicon 70% by weight
Lead Frame Material	Copper
Lead Plating Composition	Tin or solder, 300 to 800 micro inches (μin)
Die Attach Material	Silver Epoxy
Die Coat	Dow Corning Q14939 silicon gel
Bond Wire	Gold, 1.3 mil diameter
Bond Attach Method	Thermosonic
JLCC	
Body Material	Ceramic
Lid and Lead Material	Alloy 42 with minimum 60-μin gold plate
Bond Wire	99% Aluminum, 1% Si, 1.25 mil diameter
Bond Attach Method	Ultrasonic

Thermal Resistance (°C/Watt)

Package	44 PLCC	44 JLCC	68 PLCC	68 JLCC	84 PLCC	84 JLCC	84 PGA
θ_{JC}	15	5	13	5	12	5	8
θ_{JA}	52	38	45	35	44	34	35

High Temperature Operating Life (HTOL) Test

The intent of HTOL is to dynamically operate a device at high temperature (usually 125°C) and extrapolate the failure rate to typical operating conditions. This test is defined by Military Standard-883 in the Group C Quality Conformance Tests. The Arrhenius relationship in equations 3 and 4 is used to do the extrapolation. To use the Arrhenius equation, we need to know the activation energy of the failure mode. Activation energies of antifuse failure modes were discussed earlier. Table 4 gives the activation energies of general semiconductor failure modes.

Table 4. Activation Energy of CMOS Failures

Failure Mechanism	Activation Energy
Ionic Contamination	1.0 eV
Oxide Defects	0.3 eV
Hot Carrier Trapping in Oxide (Short Channels)	-0.06 eV
Silicon Defects	0.5 eV
Aluminum Electromigration	0.5 eV
Contact Electromigration	0.9 eV
Electrolytic Corrosion	0.54 eV

Six different data patterns were programmed into the 64K PROMs for HTOL testing: a diagonal of zeros (98% programmed); a diagonal of ones (2% programmed); a topological checkerboard pattern (50%); all zeros (100%); all ones (0%); and an incrementing pattern (50%). During burn-in, all addresses are sequenced through at a 1 MHz clock rate. The outputs are enabled and loaded with a 100 ohm resistor to a 2 V supply. This results in an output loading of equal to or greater than the data sheet specified limits of I_{OH} = -4 mA and I_{OL} = 16 mA. In most cases, the PROMs were burned-in at V_{CC} = 5.5 V, 125°C. However, voltage acceleration experiments were also done at 7 V, 125°C as well as at 8 V, 25°C.

The PROM is useful for antifuse reliability studies for several reasons. First of all, we can program anywhere from 0% to 100% of the antifuses although we program only 2% to 3% of the antifuses for a given design on the ACT 1010/1020 device. Also, an antifuse failure on the PROM is very noticeable, since the antifuse is directly addressed. A weak antifuse would show an AC speed drift, and a failed antifuse would read the wrong data.

To evaluate the ACT 1003/1010/1020 devices, we programmed an actual design application into each device and performed a dynamic burn-in by toggling the clock pins at a 1 MHz rate. The designs selected utilized 85% to 97% of the available logic modules and 85% to 94% of the I/Os. Outputs were loaded with 1.2 kΩ resistors to V_{DD} resulting in greater than 4 mA of sink current as each I/O toggled low. Under these conditions, each ACT 1010 typically draws about 100 mA during dynamic burn-in. Most of this current comes from the output loading while about 5 mA is from the device supply current. The thermal resistance (junction to ambient) of the 68- and 84-pin PLCC packages is about 45°C/Watt; for the JLCC packages it is about 35°C/Watt. For a 125°C burn-in, this results in junction temperatures of about 150°C for plastic packages and 145°C for ceramic packages. Most burn-in was done at 5.75 V (for voltage acceleration of the antifuse) and 125°C. Some data was taken at 5.5 V, 125°C and at 5.5 V, 150°C.

A summary of the HTOL data collected by Actel is shown in Table 5. A failure is defined as any device which shows a functional failure, exceeds data sheet DC limits, or exhibits any AC speed drift. Among the parts tested, no speed drift, faster or slower, was

observed within the accuracy of the test set-up. Failure rates at 55°C and 70°C were extrapolated by using the Arrhenius equation and a general activation energy of 0.6 eV. Poisson statistics were used to derive a calculated failure rate with a 60% confidence level. Use of Poisson statistics is valid for a failure rate which is low and a failure mode which occurs randomly with time. At 55°C, the calculated failure rate with a 60% confidence level was found to be 33 FITS (0.0033% failures per 1000 hours). This number was derived from over 2.2 million device hours of data.

Both of the observed failures were normal CMOS failures and were not caused by the antifuses. The 1003 device failed after 80 hours at 150°C. The unit was functional but had high I_{DD} current (40 mA vs. 4 mA typical). Liquid crystal analysis revealed a hot spot outside the antifuse area of the chip. The other failed unit was nonfunctional, with a high I_{DD} current of about 40 mA. This unit failed after 500 hours at 125°C. Both failures are believed to be the results of junction degradation or silicon defects.

Table 5. HTOL (High Temperature Operating Life) Test

Device	Units	Runs	Device Hours at 125°C	Failures	Equivalent Device Hours at 55°C (0.6 eV)	Equivalent Device Hours at 70°C (0.6 eV)
PROM64	275	4	568,000	0	23.8 Million	9.4 Million
1003 JLCC	238	3	359,400	1	15.0	5.9
1010 JLCC	144	6	283,000	0	11.8	4.7
1020 JLCC	61	2	90,000	0	3.8	1.5
1020A JLCC	69	2	69,000	0	2.9	1.1
1010 PLCC	496	6	844,000	1	35.3	14.0
1020 PLCC	32	2	48,000	0	2.0	0.8
Totals:	**1315**	**20**	**2,261,400**	**2**	**94.6 Million**	**37.4 Million**

Summary:	
Observed FITS at 55°C:	21
Observed FITS at 70°C:	53
Calculated FITS to 60% confidence at 55°C:	33
Calculated FITS to 60% confidence at 70°C:	83

(Summary of Data as of February 20, 1990)

Unbiased Steam Pressure Pot Test

This test is used to qualify products in plastic packages. Units are placed in an autoclave (pressure pot) and exposed to a saturated steam atmosphere at 121°C and 15 psi. Problems with bonding, molding compounds, or wafer passivation can cause metal corrosion to occur in this atmosphere. Metal corrosion is detected during a full electrical test of the device following exposure to the autoclave environment.

A total of 426 units from five wafer runs and six assembly lots were used. Read points were taken at 96, 168, and 336 hours. There were a total of four failures (Table 6). All four failures were caused by bond wires lifting off bond pads. This was an assembly problem that occurred only on our first lot of plastic units. The failures were caused by high temperature, not by metal corrosion. The assembly problem was corrected, with no further failures observed.

Table 6. Unbiased Steam Pressure Pot Test
121°C, 15 psi

Product	Run Number	Package	Number of Units	Number of Failures		
				96 Hours	168 Hours	336 Hours
1010	JB13	84 PLCC	34	0	3	0
1010	JB13	68 PLCC	71	1	0	0
1010	JB14	68 PLCC	71	0	0	0
1010	JB22	68 PLCC	71	0	0	0
1010	JB27	68 PLCC	50	0	0	0
1010A	TI24	68 PLCC	129	0	0	0

Biased Moisture Life Test (85/85)

In this test, the units are placed in a chamber at a temperature of 85°C and a relative humidity of 85%. A voltage of 5.5 V is applied to every other device pin while other pins are grounded. 5.5 V is applied to V_{DD} while V_{SS} is grounded. This test is effective at detecting die related and plastic package related problems.

As shown in Table 7, a total of 288 units were stressed. There were three failures. One failure was caused by two lifted bond wires; it was from the same lot in which we saw failures in steam pressure pot test. The second unit was functional but had high I_{DD} current. The 1000-hour failure was nonfunctional.

Table 7. Biased Moisture Life Test
85°C/85% Humidity with DC Alternate Pin Bias of 0 V to 5.5 V

				Number of Failures		
Product	Run Number	Package	Number of Units	500 Hours	1000 Hours	2000 Hours
1010	JB13	68 PLCC	80	2	1	0
1010	JB14	68 PLCC	81	0	0	0
1010	JB22	68 PLCC	54	0	0	–
1010	JB26	68 PLCC	54	0	0	–
1010	JB27	68 PLCC	19	0	0	–

Temperature Cycling

This test checks for package integrity by cycling units through temperature extremes. For ceramic packages, the range of temperature is –65°C to 150°C. For plastic packages, the range is 0°C to 125°C. Both programmed and unprogrammed units are placed on temperature cycle. Data on 451 units is summarized in Table 8.

Table 8. Temperature Cycling Test
–65°C to 150°C Ceramic; 0°C to 125°C Plastic

				Failures		
Product	Run Number	Package	Number of Units	100 Cycles	200 Cycles	1000 Cycles
1010	JB13	68 PLCC	158	0	–	0
1010	JB14	68 PLCC	28	0	–	0
1010	JB26	68 PLCC	21	0	–	0
1010	JB28	68 PLCC	31	0	–	0
1020	JB22	84 PLCC	17	0	–	0
1010	1077	84 JLCC	20	0	0	
1020	JB33	84 PGA	25	0		
1010A	TI24	68 PLCC	176	0	–	0

Other Tests

Electrostatic Discharge (ESD)

Units were tested for sensitivity to static electricity by using the human body model as described in MIL-883C (100 pF discharged through 1.5 kΩ). Fifteen ACT 1010 units from three wafer runs were tested. Nine representative I/O pins were checked on each device. Since all I/O pins have the same layout on the chip, the nine pins tested were selected based on their proximity to V_{SS}, V_{DD}, or the corner of the chip. The MODE pin was also tested because it is the only dedicated input on the chip. In addition, the three power supplies (V_{SS}, V_{DD}, V_{PP}) were tested. Three positive and three negative pulses were discharged into each pin tested at each voltage level. For inputs and I/Os, these six pulses were applied with three different grounding conditions: V_{SS} only grounded, V_{DD} only grounded, and all other I/Os grounded. Thus each pin received a total of eighteen pulses for each test voltage. Testing began at 1000 V and continued in 500 V increments. After pulsing was completed at each voltage, the I-V characteristic of each pin was checked on a digital curve tracer. Any significant change in the I-V curve from the previous reading was considered a failure. The units were then tested on a VLSI tester. Leakage currents were datalogged at 0 V and 5.5 V. Any pin showing more than 250 nA of leakage current was also considered to be a failure. For I_{DD}, a change of more than 250 μA was cause for rejection. No failures occurred through 2000 V. At 2500 V, five of the fifteen units failed on at least one pin. Failure analysis revealed that the failures occurred on the N-channel pulldown transistor of the output driver. With no failures through 2000 V testing, the ACT 1010 (and the ACT 1020, by virtue of identical I/O layout to the 1010 device) met the requirements for the 2000 V ESD category of MIL-883C.

Latch-up

Latch-up is a well-known cause of failure in CMOS circuits. Parasitic bipolar transistors are created by the P-channel transistor, the N-channel transistors, the N-well, and the P-substrate. These transistors are connected in a manner which effectively creates an SCR. If a voltage on an external pin were to forward bias to the substrate, the parasitic SCR can be latched to the on state, creating a low-impedance path between V_{DD} and ground. A large amount of current then flows through this path. This current can, at best, make the device temporarily nonfunctional and, at worst, cause permanent damage.

Several techniques are used by CMOS designers to reduce the chance of latch-up. One of the most common techniques is the use of guard rings to isolate P-channel and N-channel transistors. The disadvantage of this method is that it requires additional silicon die area. Another method is to use a substrate bias generator. Creating a negative substrate bias means that an input must go even more negative to cause latch-up. A third technique is to use EPI wafers to achieve low substrate resistance, which lowers the chances of triggering latch-up. Actel designers use both guard ring and EPI wafer techniques for ACT 1010/1020 devices.

The latch-up test method used is defined by JEDEC Standard No. 17. Each I/O pin on a tested device was forward biased in both directions (to V_{SS} and V_{DD}) by forcing negative and positive currents ranging from ±50 mA to ±250 mA in 50 mA increments. Following each stress, the device I_{DD} current was measured. If the current exceeded the data sheet limit of 10 mA, the unit would be rejected. The device was also functionally tested.

Fifteen units from three different wafer lots were tested. Testing was done both at room temperature and at a worst case temperature of 135°C. All device I/Os and power supplies were tested. No failures were detected through 250 mA.

Conclusion

The data presented in this report establishes the excellent reliability of Actel ACT 1010/1020 devices. Both the Actel models and the test devices show that the antifuse is highly reliable and that it detracts negligibly from overall product reliability.

References

1) E. Hamdy, et al, *"Dielectric Based Antifuse for Logic and Memory ICs."* IEDM paper, p. 786-789, 1988.

2) S. Chiang, et al, *"Oxide-Nitride-Oxide Antifuse Reliability."* To be published, Proc. Int. Rel. Phys. Symp., 1990.

3) J. Lee, I-Chen, and C. Hu, *"Modeling and Characterization of Gate Oxide Reliability,"* IEEE Trans. of Elec. Dev., Dec. 1988.

Device Resources

Device	Modules	Gates	User I/Os			
			84 JQCC	68 JQCC	44 JQCC	84 PGA
1010	295	1200	N/A	57	34	57
1020	546	2000	69	57	34	69

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Note:

1. $V_{PP} = V_{CC}$, except during device programming.

Recommended Operating Conditions

Parameter	Military	Units
Temperature Range (T_C)	-55 to +125	°C
Power Supply Tolerance	±10	%V_{CC}

Power Dissipation

The following formula is used to calculate total device dissipation.

Total Chip Power (mW) = 0.41 N*F1 + 0.17 M*F2 + 1.62 P*F3

Where:

F1 = Average logic module switching rate in MHz.

F2 = Average clock pin switching rate in MHz.

F3 = Average I/O switching rate in MHz.

M = Number of logic modules connected to the clock pin.

N = Total number of logic modules used on the chip. (including M)

P = Number of outputs used loaded with 50 pF.

The second term, variables F2 and M, may be ignored if the CLKBUF macro is not used in the design.

DC Characteristics

V_{CC} = 5.0 V ± 10%, -55 °C ≤ T_C ≤ +125 °C

Symbol	Parameter	Test Conditions	Group A Subgroups	Limits Min.	Limits Max.	Units
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 4 mA Test one output at a time	1, 2, 3		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = -3.2 mA Test one output at a time	1, 2, 3	3.7		V
V_{IL}	Input Low Level		1, 2, 3	-0.3	0.8	V
V_{IH}	Input High Level		1, 2, 3	2.0	V_{CC} + .3	V
I_{CC}	Standby Supply Current	V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND Outputs unloaded	1, 2, 3		25	mA
I_{IL}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND	1, 2, 3	-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = 5.5 V, V_{OUT} = V_{CC} or GND	1, 2, 3	-10	10	µA
I_{OS}	Output Short Circuit Current V_{OUT} = V_{CC}	Test one output at a time	1, 2, 3	20	140	mA
	V_{OUT} = GND	V_{CC} = 4.5 V for min. limit V_{CC} = 5.5 V for max. limit		-10	-100	mA

Switching Characteristics

V_{CC} = 5.0 V ± 10%, -55 °C ≤ T_C ≤ +125 °C

Symbol	Parameter	Test Conditions	Group A Subgroups	Limits Min.	Limits Max.	Units
t_{PDB}	Binning Circuit Delay ACT 1010	V_{CC} = 4.5 V V_{IL} = 3 V, V_{IL} = 0 V V_{OUT} = 1.5 V	9, 10, 11		120	ns
	ACT 1020				186	ns

Functional and Switching Tests

ACT 1010 and ACT 1020 devices can be tested functionally by using a serial scan test method. Data is shifted into the SDI pin, and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the modules can be read by shifting out the output response. All units are tested for functionality over the military temperature range. Group A subgroups 7, 8A, and 8B are tested in the same manner.

AC timing for logic module internal delays and pin-to-pin delays is determined after place and route. The ALS Timer utility displays actual timing parameters for circuit delays. Since these delays are design-dependent and cannot be tested on unprogrammed devices, Actel tests for AC performance by measuring the input-to-output delay of a special path called the "binning circuit."

The binning circuit consists of one input buffer + n logic modules + one output buffer (n = 16 for the ACT 1010; n = 28 for the ACT 1020). The logic modules are distributed along two sides of the device. These modules are configured as inverting and non-inverting buffers. The modules are connected through programmed antifuses with typical capacitive loading.

Actel uses a special benchmark design to correlate the binning circuit delay to typical and worst-case design delays. Samples of units are programmed to this benchmark circuit and all programmed paths are measured for AC performance (including the binning circuit delay). The measured delays are then compared to the ALS Timer predictions. The binning circuit maximum delay has been set to assure conformance to the predicted delays. Units are sampled to confirm this correlation upon initial device characterization and whenever a change is made that may affect AC performance.

Package Thermal Characteristics

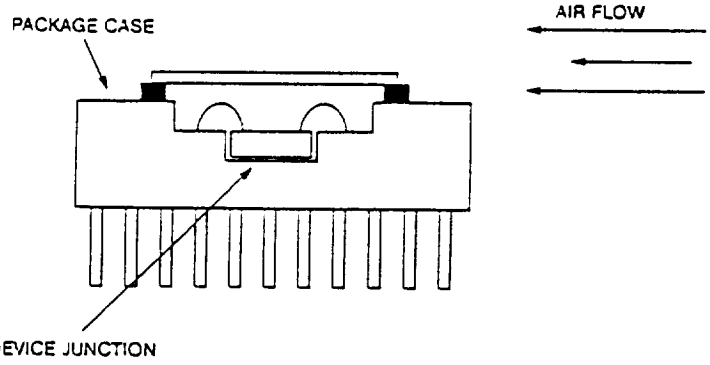
The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for a ceramic PG84 package at military temperature is as follows:

150 (Max) - 125 (Max Mil.) = 25/33 C/W (PG84 - still air) = 0.76 Watts.

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Ceramic Pin Grid, PG84	84	8	33	20	°C
Cerquad J lead, JQ44	44	8	40	32	°C
Cerquad J lead, JQ68	68	8	38	30	°C
Cerquad J lead, JQ84	84	8	36	25	°C



SECTION 2.4
Calculation of Current Density

JET PROPULSION LABORATORY

February 14, 1992

SUBJECT: CALCULATION OF CURRENT DENSITY FOR ACTEL 2.0um TECHNOLOGY

PURPOSE: To review the issue of current density and worst case metal step coverage according to Mil-Std-883 and Mil-M-38510 requirements. Both of these requirements are to be evaluated at worst case conditions. Worst case conditions will vary according to process technology and individual part performance. Therefore a best approximation to worst case conditions is used for current density calculations and time to failures. Step coverage is measured from SEM photographs which represent worst case topology on a chip.

PROCEDURE:

1.0. Figure 1 is a SEM photograph and cross section which shows a metal-1 contact to silicon and the thinning of the metal from a nominal of 0.85um to a minimum of 0.2um. This is a violation which can lead to metal failure due to electromigration under certain conditions. The minimum contact size is designed as 1.8x1.8um. In actuality it becomes smaller due to processing and the metal thins out at the sidewalls.

2.0 Figure 2 is an optical photograph of a partial chip deprocessed down to silicon showing poly and contacts.The feature to note is that the number of contacts observed on silicon varies from one to as many as sixteen depending on the size of transistor geometry. The concern is if there is only one contact to the drain or source of the transistor. This is worst case for current flow. The amount of current will depend on the size of the transistor and its function in the circuit. One contact maximizes current density. Two or more contacts will lower current density since the current will be shared.

3.0 Figure 3 is the physical model used to represent the metalization entering the contact or a via. The concern is the thinning of the metal within the contact. This model was used to calculate the metal-1 area as it thins within the contact. This area is represented by A1.

4.0 Figure 4 is the mathematical model used to calculate current density and the predicted time to failure shown in hours and years. The model calculates for three cases: 1) single contact which is worst case, 2) two contacts which reduces current density, 3) no contact in metal interconnect which is the best case. From these three cases it is easy to compare results and reach some conclusion. This model also shows the entered variables that were used to represent worst case process and worst case transistor rating. This is an interactive model so any enter variable can be changed to study the effect. The significant variable is the current value chosen to represent worst case in the transistor. ACTEL's data book quotes 4ma minimum for output buffers. They also claim the current for the 1.2um technology is 1.0ma per contact which is what was assumed for the 2.0um. This analysis assumes dc current flow.

5.0 Figure 5 shows current density as metal-1 thickness increases. As expected the current density is reduced as metal thickness increases. This figure also shows that two contacts reduce it further because of current sharing. From a design/reliability point of view more than one contact should be used where possible.

6.0 Figure 6 shows time to failure as metal-1 thickness increases. The step coverage is critical to insuring maximum time to failure. Two contacts are added insurance.

7.0 Figure 7 shows the time to fail for a single contact vs metal thickness on a magnified scale. This figure shows .01% failures in metal-1 are predicted to occur in less than 10 years operating at temperature of 150°C.

8.0 Figure 8 shows time to fail can be increased by lowering the operating temperature.

Conclusions: The ACTEL 2.0 um technology does not meet Mil-Std-883 metal contact step coverage requirement of 30% for contacts less than 3um on a side using worst case SEM examination. However it does pass the Mil-M-38510 current density requirement of 2x10E5 A/cm2 even when the metal-1 step coverage is 23.5%. This is because the current flow allowed by design is 1ma per contact for the 1.2um technology. This 1ma per contact was also assumed for the 2.0um calculations.

Therefore based on the calculations performed a mission of 5 years or less has minimum risk if the device max junction temperature will remain below 90°C. This temperature allows for current and step coverage variations. Beyond 5 years the risk is greater that electromigration or other metal failures may occur since there are places on the chip where only one contact is used.

Further action should investigate why additional contacts were not used when it seems there is physical room for them. If there is a design or routing limitation then the risk will remain for lack of redundancy. In this case only improving the metal-1 step coverage will reduce the risk.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE PATTERNS ON Si SUBSTRATE.

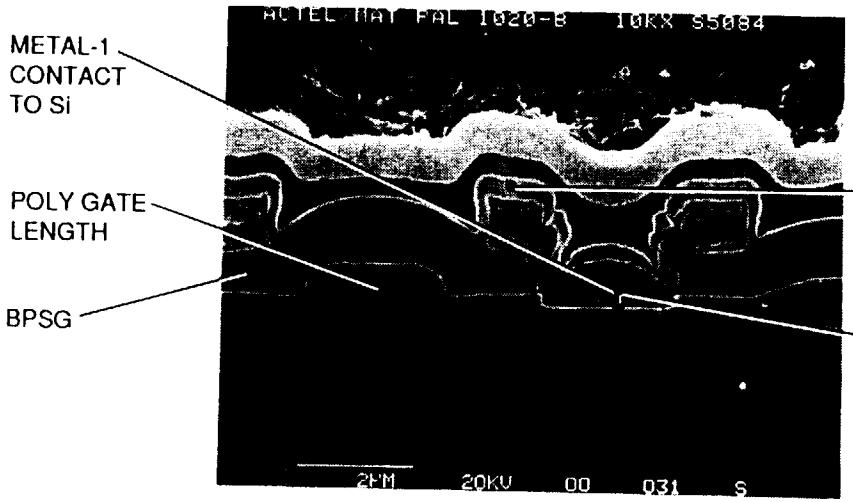


Figure 1a. 10kX view of metal-1 contact to Si, and poly gate length pattern on gate oxide.

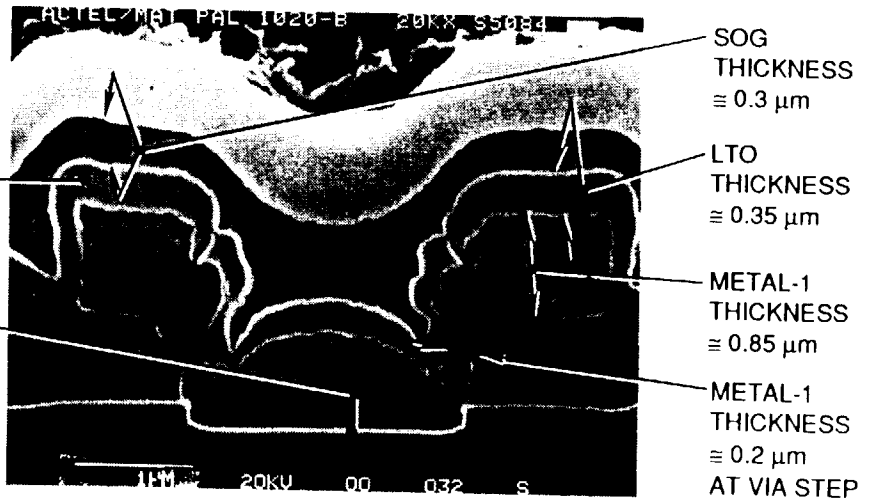


Figure 1b. 20kX view of metal contact to Si, and metal step coverage thickness in BPSG via sidewall cut.

OPTICAL PHOTOVIEWS OF ACTEL 1020B(2um PROCESS) CHIP SEGMENT

EXPOSED CONTACTS TO POLY GATES AND Si-TRANSISTOR CELLS
(DIELECTRICS AND 2-LEVEL METAL INTERCONNECTIONS REMOVED)

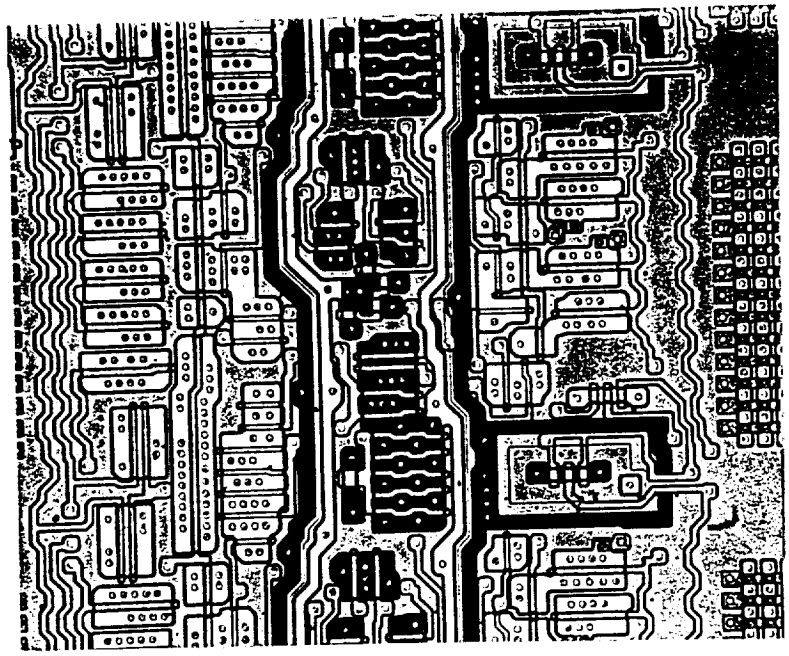
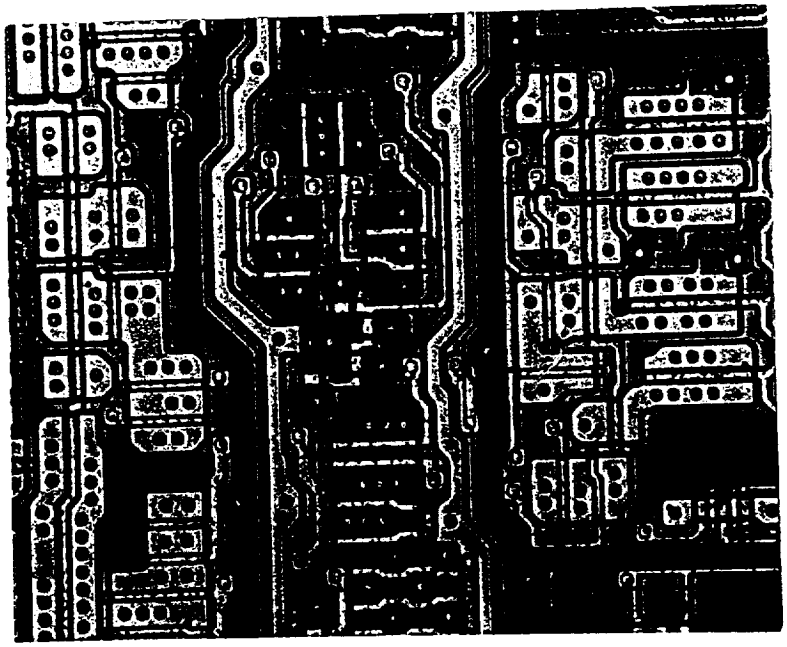


FIGURE 2A
500X OPTICAL VIEW OF EXPOSED CONTACTS TO POLY AND Si-TRANSISTORS



SINGLE
CONTACTS
TO Si ARE SEEN

FIGURE 2B
800X OPTICAL VIEW OF EXPOSED CONTACTS TO Si CELLS

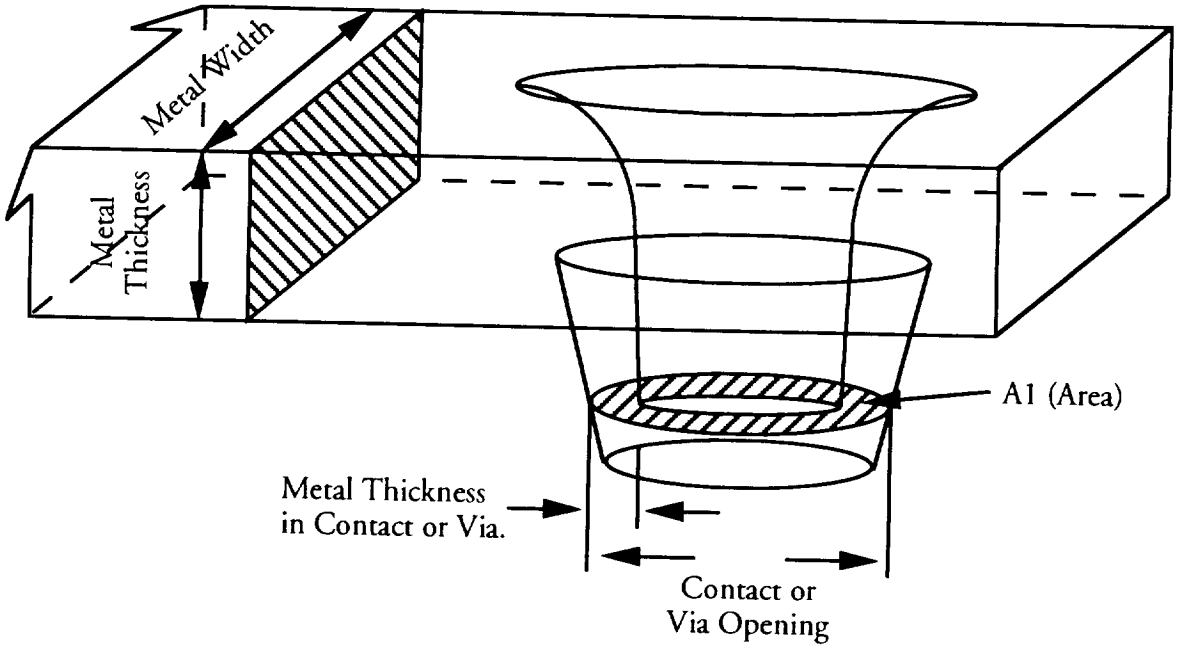


Figure 3
Transparent view of metallization entering via (or contact) opening

JET PROPULSION LABORATORY
M.Sandor

Vendor: Actel

CURRENT DENSITY CALCULATION FOR SINGLE OR MULTIPLE CONTACTS FROM METAL 1 TO SILICON

Technology:CMOS 2um; Metal 1 is AL-Si(1%)-Cu(0.5%); LOCOS Passivation is 300nm SiO2,800 nm SiN

	Enter	Unit	Calculation	
Metal 1width	4.00	um		
Metal 1 thickness	0.85	um	A1 in cm2 =	9.4248E-09
			CD@A1 =	1.06E+05
Contact opening size (oxide)	1.8	um		
Contact size at A1(Silicon)	1.70	um	A1 in um2 =	0.94248
Metal 1 thickness at step	0.20	um		
Step coverage at contact (edge ratio)			23.5%	
Step coverage at contact (conical ratio)			27.72%	
Worst case current in metal 1(derated) (out buffers are rated at 4.0ma)	1.00	ma		
Temperature(max operationg +Junct rise)	150	Cent		
Nominal capacitance	7.00	pf		
VDD	5.50	Volts		
Switching period of device	45.00	ns		
Frequency of device			22.22	Mhz
Case 1:Current density in single contact [This is worst case]			1.06E+05	A/cm2
			1.06	ma/um2
Case 2: C.D. with multiple contacts [This is typical case]	2	cts.	5.31E+04	A/cm2
Case 3: C.D. w/o conts. (interconnect) [This is best case]			2.94E+04	A/cm2
Case 1: Current density in single contact (alternate calculation method: Jmax=(1.2xCxVdd)/(periodxA1)			1.09E+05	A/cm2

t50 and t.01 TIME TO FAILURE (for log-normal distribution)
where t.50 = A.50*J^-n*exp(Ea/KT) [BLACK'S EQUATION]

	Enter	Unit	Calculation Unit
A50(constant) =	5.00E+07	hrs	A.01(constant 1.39E+07 hrs
n(current density exponent) =	2		where A.01 = A50*e(sigma*Z)
k(Boltzmann constant) =	8.62E-05	ev/K	sigma of failure distribution = ln(t.50/t.16)/1
T(temperature) =	423	K	Z = from statistics table
Ea(activation energy for EM) = [for Al-Si-Cu]	0.63	ev	

Current density in single contact [This is worst case]	=	1.06E+05	A/cm2;	t50 = 142309 hrs 16.2 yrs **t.01 = 39508 hrs 4.5 yrs**
Reduced C.D. with multiple contacts [This is typical case]	=	5.31E+04	A/cm2;	t50 = 569235 hrs 65.0 yrs t.01 = 158031 hrs 18.0 yrs
Current density interconnect [This is best case]	=	2.94E+04	A/cm2;	t50 = 1852019 hrs 211.4 yrs t.01 = 514158 hrs 58.7 yrs

Case 1[Duty cycle = .50]
t50(pulse) = 65.0 yrs
t.01(pulse) = 18.0 yrs

Figure 4

Jet Propulsion Laboratory
M.Sandor

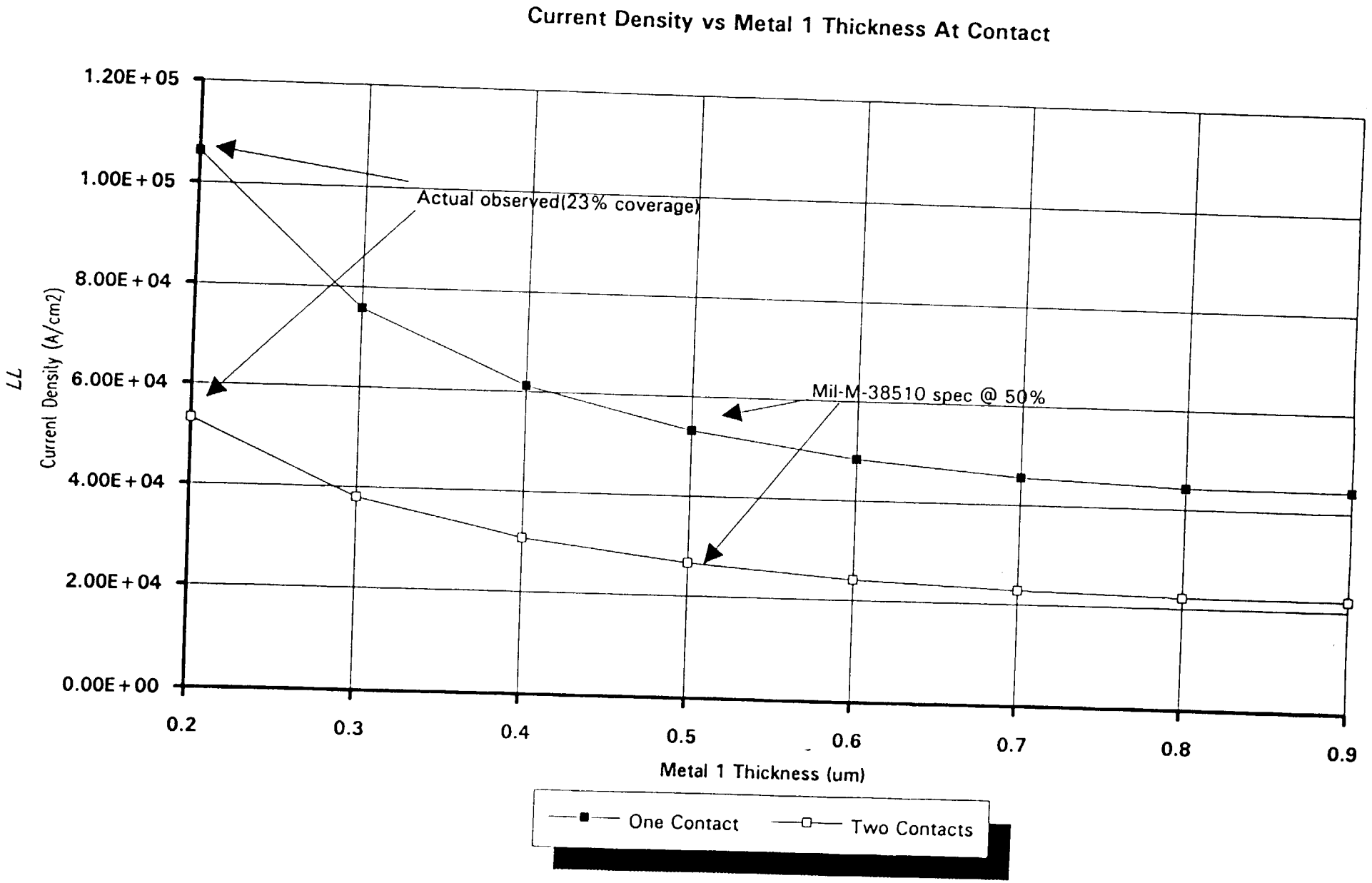


Figure 5

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METAL 1 TIME TO FAIL (t.01) for ELECTROMIGRATION

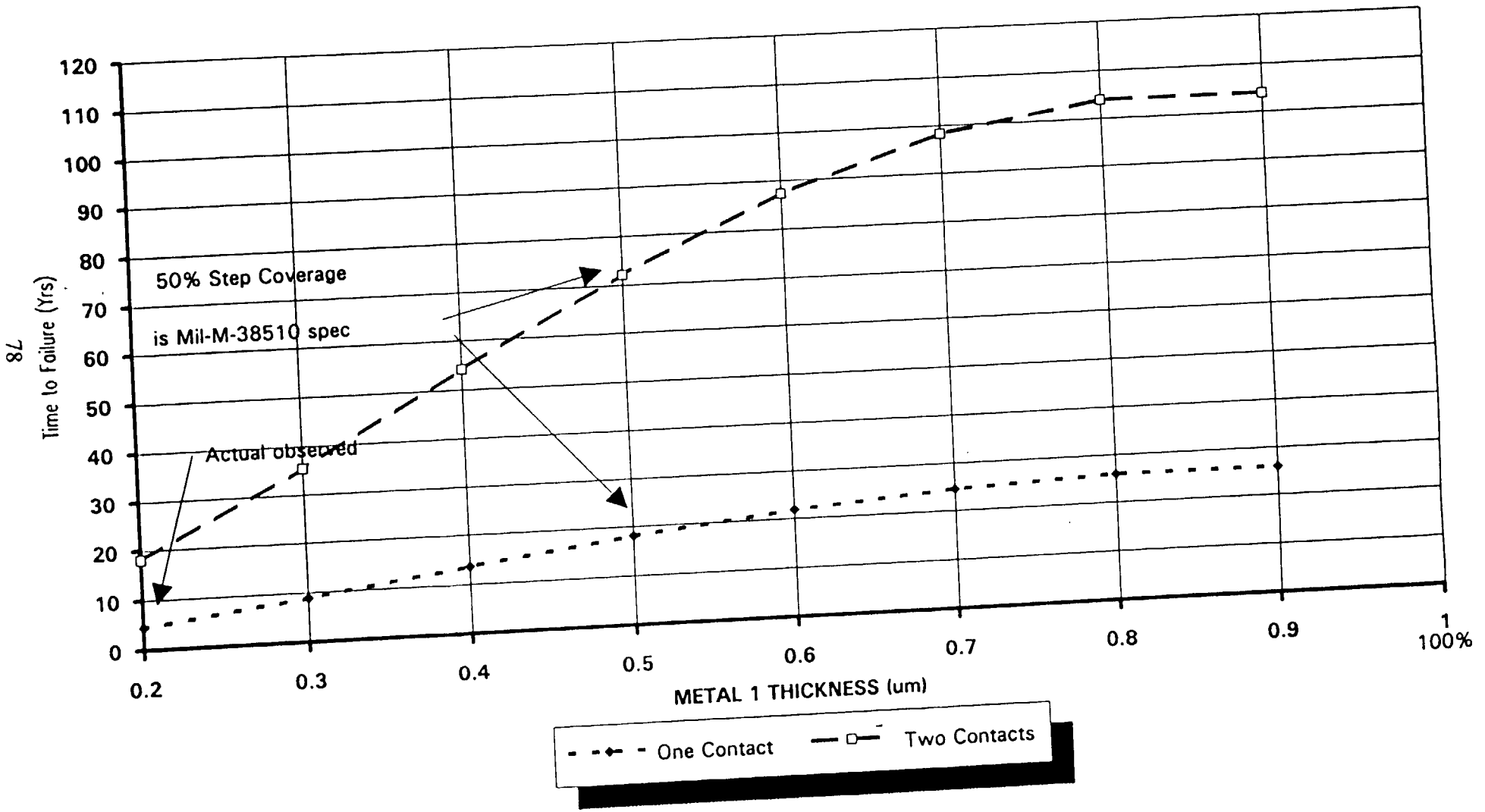

Figure 6

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M.Sandor

METAL I TIME TO FAIL (t.01) for ELECTROMIGRATION

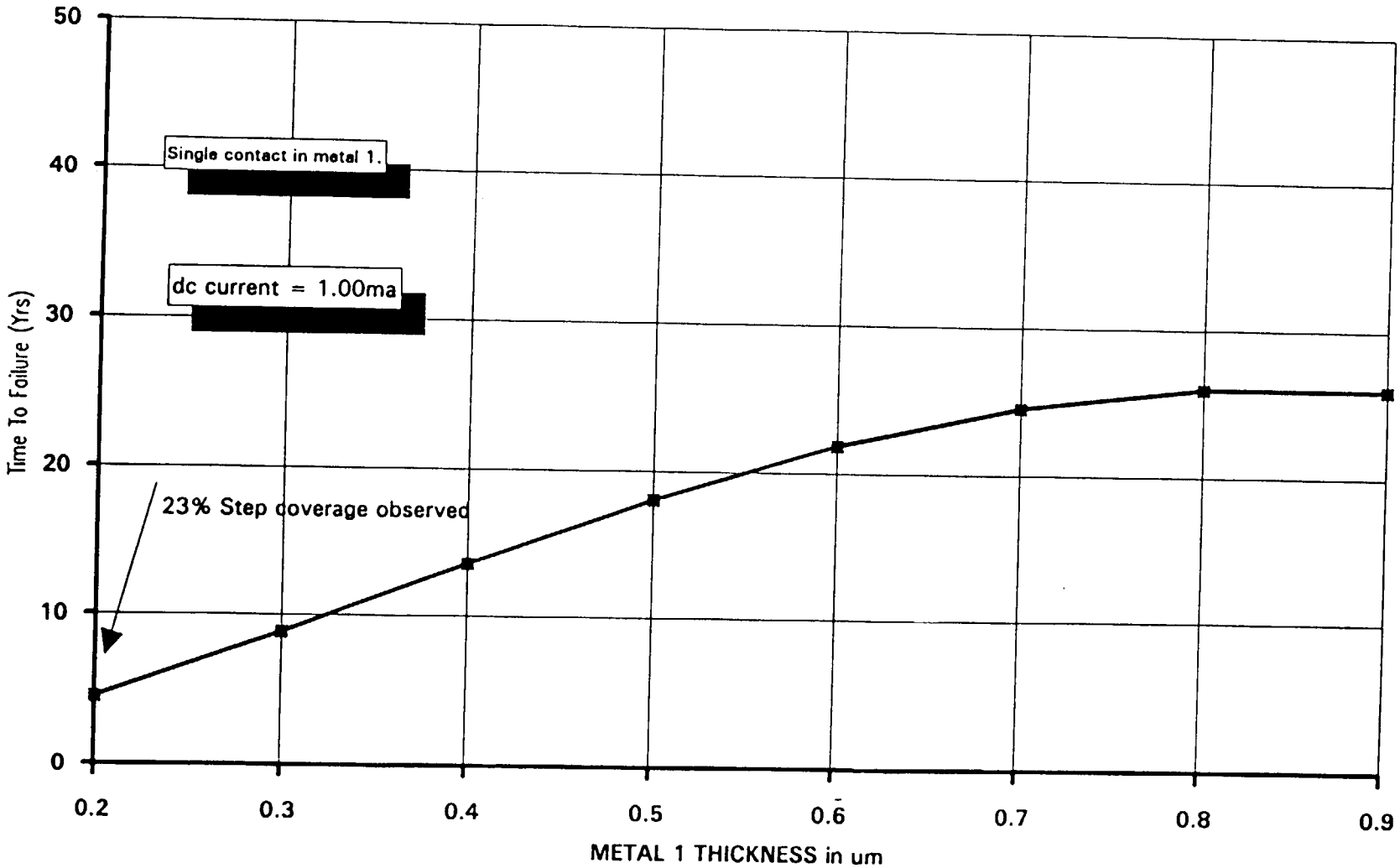

Figure 7

JET PROPULSION LABORATORY
M.SANDOR

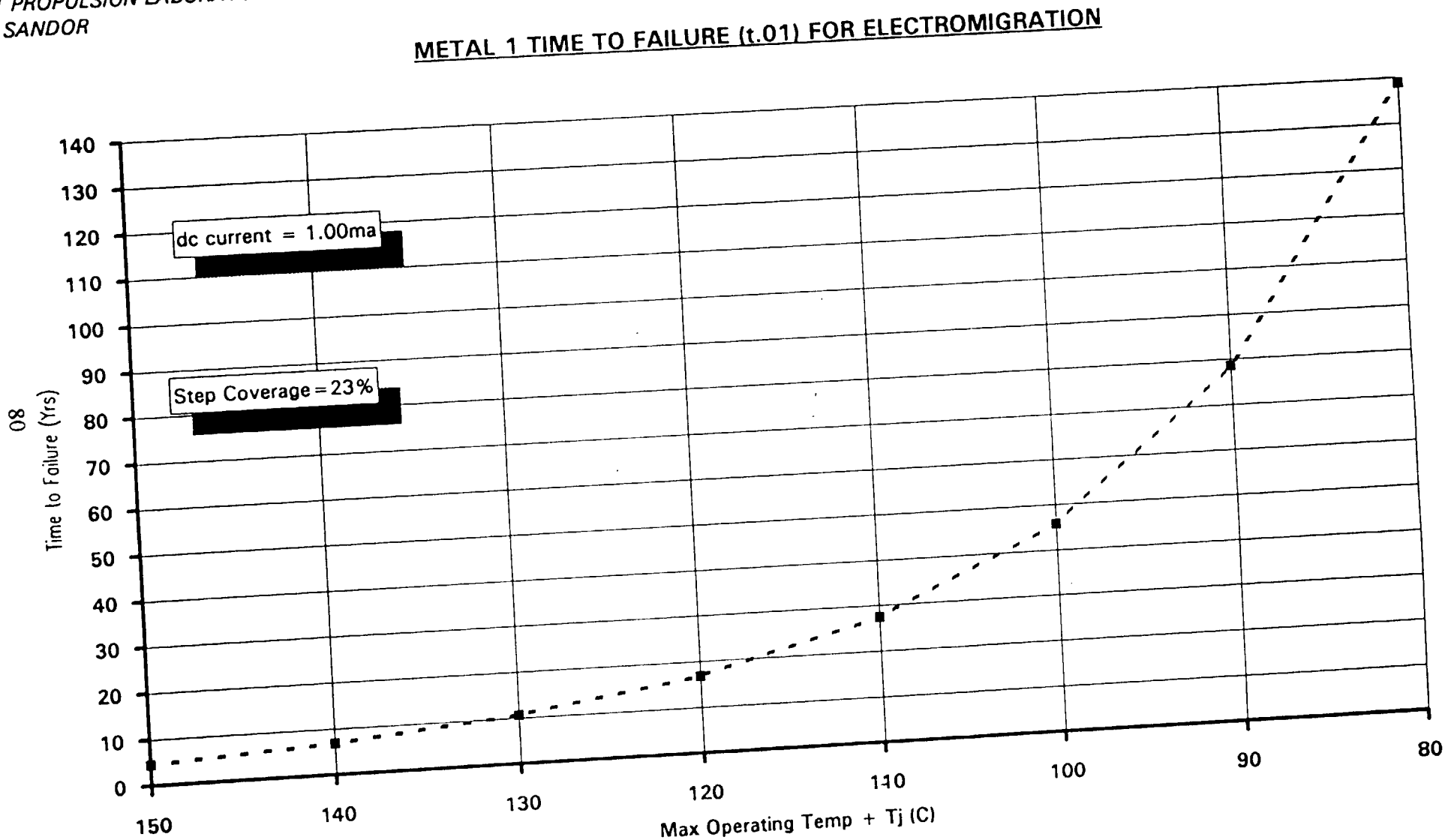

Figure 8

JET PROPULSION LABORATORY
M.SANDOR

METAL 1 TIME TO FAILURE (t.01) FOR ELECTROMIGRATION

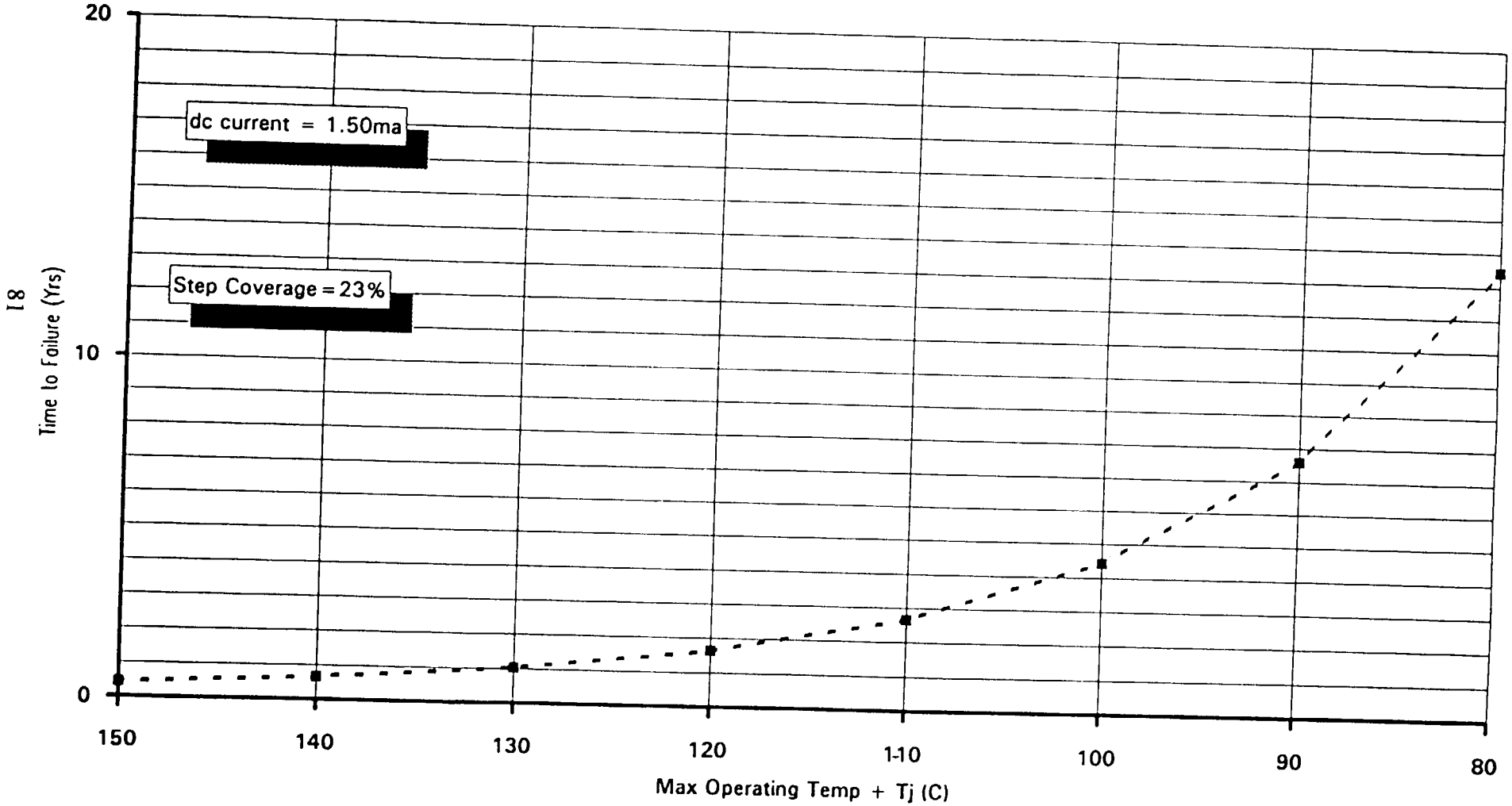

Figure 8A

SECTION 2.5
Electrical Characterization Data

Example

JPL Alpha-11 A1020 FPGA
03-APR-1992 17:55:56.59 Datecode: 9129 Temp: 25 Ser #: 10
Source file: alpha11.C:H35 Page: 1
Endpoint: 2000hrs

Functional test params: Vcc = 4.50V, Vih = 3.00V, Vil = 0.00V.

Functional test params: Vcc = 4.75V, Vih = 3.00V, Vil = 0.00V.

Functional test params: Vcc = 5.00V, Vih = 3.00V, Vil = 0.00V.

Functional test params: Vcc = 5.25V, Vih = 3.00V, Vil = 0.00V.

Functional test params: Vcc = 5.50V, Vih = 3.00V, Vil = 0.00V.

VOH Params: Ins = 3.00V/0.00V, IO = -3.200MA, Min = 3.7

VCC	4.5	4.75	5	5.25	5.5
Q0	4.2025	4.4667	4.7285	4.9878	5.2471
Q1	4.2001	4.4643	4.726	4.9829	5.2422
Q2	4.2001	4.4618	4.7236	4.9829	5.2397
Q3	4.1854	4.4472	4.7065	4.9658	5.2226
FF1	4.2025	4.4667	4.726	4.9853	5.2446
FF2	4.2074	4.4692	4.7309	4.9902	5.2471
TOUT1	4.1952	4.4569	4.7187	4.978	5.2373
TOUT5	4.1977	4.4594	4.7211	4.9804	5.2397
DCE0	4.1977	4.4618	4.7211	4.9829	5.2397
DCE1	4.2001	4.4643	4.726	4.9853	5.2446
DCE2	4.2025	4.4667	4.7285	4.9853	5.2446
DCE3	4.1977	4.4594	4.7236	4.9804	5.2397
DCE4	4.2074	4.4716	4.7309	4.9902	5.2471
DCE5	4.2025	4.4667	4.7285	4.9853	5.2446
DCE6	4.205	4.4692	4.7285	4.9878	5.2471
DCE7	4.2074	4.4692	4.7309	4.9902	5.2495
DCE8	4.205	4.4692	4.7285	4.9878	5.2471
DCE9	4.2074	4.4692	4.7309	4.9902	5.2471
DCE10	4.2074	4.4692	4.7285	4.9902	5.2446
DCE11	4.2025	4.4643	4.726	4.9853	5.2397
DCE12	4.2001	4.4618	4.7236	4.9829	5.2397
DCE13	4.2001	4.4643	4.7236	4.9829	5.2422
DCE14	4.1977	4.4618	4.7236	4.9804	5.2373
DCE15	4.2025	4.4643	4.7211	4.9829	5.2397
DCE16	4.1977	4.4594	4.7211	4.9804	5.2397
DCE17	4.1977	4.4594	4.7236	4.9804	5.2397
DCE18	4.1977	4.4594	4.7211	4.9829	5.2397
DCE19	4.2001	4.4643	4.7236	4.9853	5.2422
DCE20	4.1952	4.4618	4.7211	4.9804	5.2397
DCE21	4.1928	4.4569	4.7187	4.978	5.2373
DCE22	4.1952	4.4569	4.7211	4.9804	5.2397
DCE23	4.1977	4.4594	4.7211	4.9804	5.2397
DCE24	4.1928	4.4569	4.7187	4.978	5.2373
DCE25	4.1977	4.4594	4.7211	4.9804	5.2397
DCE26	4.2001	4.4618	4.7211	4.9829	5.2422
DCE27	4.1952	4.4594	4.7211	4.9804	5.2373
DCE28	4.1952	4.4594	4.7187	4.978	5.2348
DCE29	4.183	4.4447	4.7016	4.9609	5.2177
DCE30	4.1928	4.4545	4.7162	4.9731	5.2324
DCE31	4.1903	4.4521	4.7114	4.9731	5.2299
DCE32	4.2074	4.4692	4.7309	4.9902	5.2495
DCE33	4.205	4.4667	4.7285	4.9878	5.2446

DCE34	4.2074	4.4667	4.7285	4.9878	5.2446
DCE35	4.2074	4.4692	4.7309	4.9902	5.2471
DCE36	4.1977	4.4643	4.7211	4.9829	5.2397
DCE37	4.2025	4.4643	4.726	4.9853	5.2422
DCE38	4.2025	4.4667	4.726	4.9853	5.2446
DCE39	4.2074	4.4692	4.7309	4.9902	5.2495
MOUT40	4.1952	4.4569	4.7187	4.978	5.2373
MOUT41	4.1928	4.4545	4.7162	4.9755	5.2348
MOUT42	4.1854	4.4472	4.7016	4.9609	5.2177
MOUT43	4.1854	4.4447	4.704	4.9584	5.2153
MOUT44	4.1805	4.4398	4.6991	4.956	5.2104
MOUT45	4.2025	4.4643	4.7236	4.9829	5.2422
MOUT46	4.1977	4.4594	4.7187	4.978	5.2348
MOUT47	4.1977	4.4594	4.7187	4.978	5.2348

VOL Params: Ins = 3.00V/0.00V, IO = 4.000mA, Max = 400mv/Min = 0.0

VCC	4.5	4.75	5	5.25	5.5
Q0	1.15E-01	1.13E-01	1.15E-01	1.08E-01	1.05E-01
Q1	1.13E-01	1.10E-01	1.08E-01	1.03E-01	1.03E-01
Q2	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
Q3	1.15E-01	1.10E-01	1.08E-01	1.05E-01	1.05E-01
FF1	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
FF2	1.15E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
TOUT1	1.17E-01	1.13E-01	1.10E-01	1.05E-01	1.05E-01
TOUT5	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE0	1.15E-01	1.10E-01	1.08E-01	1.03E-01	1.03E-01
DCE1	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE2	1.20E-01	1.15E-01	1.13E-01	1.08E-01	1.05E-01
DCE3	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.03E-01
DCE4	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE5	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE6	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE7	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE8	1.15E-01	1.13E-01	1.10E-01	1.05E-01	1.03E-01
DCE9	1.17E-01	1.15E-01	1.10E-01	1.05E-01	1.05E-01
DCE10	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE11	1.15E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE12	1.15E-01	1.13E-01	1.10E-01	1.05E-01	1.03E-01
DCE13	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.03E-01
DCE14	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE15	1.15E-01	1.13E-01	1.08E-01	1.08E-01	1.03E-01
DCE16	1.15E-01	1.13E-01	1.08E-01	1.05E-01	1.03E-01
DCE17	1.15E-01	1.10E-01	1.08E-01	1.03E-01	1.03E-01
DCE18	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE19	1.20E-01	1.15E-01	1.13E-01	1.08E-01	1.05E-01
DCE20	1.20E-01	1.17E-01	1.15E-01	1.10E-01	1.08E-01
DCE21	1.17E-01	1.13E-01	1.10E-01	1.05E-01	1.05E-01
DCE22	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE23	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.03E-01
DCE24	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE25	1.17E-01	1.15E-01	1.13E-01	1.08E-01	1.08E-01
DCE26	1.20E-01	1.15E-01	1.13E-01	1.10E-01	1.08E-01
DCE27	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE28	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
DCE29	1.20E-01	1.15E-01	1.13E-01	1.10E-01	1.08E-01
DCE30	1.17E-01	1.13E-01	1.10E-01	1.05E-01	1.05E-01
DCE31	1.20E-01	1.15E-01	1.13E-01	1.10E-01	1.08E-01
DCE32	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE33	1.15E-01	1.13E-01	1.10E-01	1.05E-01	1.05E-01
DCE34	1.15E-01	1.13E-01	1.10E-01	1.08E-01	1.03E-01
DCE35	1.15E-01	1.13E-01	1.08E-01	1.05E-01	1.03E-01
DCE36	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
DCE37	1.20E-01	1.15E-01	1.13E-01	1.08E-01	1.05E-01
DCE38	1.20E-01	1.15E-01	1.10E-01	1.08E-01	1.08E-01

DCE39	1.20E-01	1.17E-01	1.15E-01	1.10E-01	1.08E-01
MOUT40	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
MOUT41	1.15E-01	1.13E-01	1.10E-01	1.05E-01	1.03E-01
MOUT42	1.15E-01	1.10E-01	1.08E-01	1.05E-01	1.03E-01
MOUT43	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
MOUT44	1.17E-01	1.13E-01	1.10E-01	1.08E-01	1.05E-01
MOUT45	1.17E-01	1.15E-01	1.10E-01	1.08E-01	1.05E-01
MOUT46	1.17E-01	1.13E-01	1.10E-01	1.05E-01	1.03E-01
MOUT47	1.17E-01	1.13E-01	1.08E-01	1.08E-01	1.03E-01

Isb Params: Ins = 3.00V, Outs = Open, Max = 25e-3, Min = 0

VCC	4.5	4.75	5	5.25	5.5
vcc	5.96E-03	8.44E-03	1.10E-02	1.33E-02	1.48E-02

IIL Params: Vin = 0.00V, Min = -10UA/Max = 10UA

VCC	4.5	4.75	5	5.25	5.5
RESET	0	-1.22E-10	-1.83E-10	-6.10E-11	0
OE	-1.22E-10	6.10E-11	0	0	-6.10E-11
LOAD	-6.10E-11	-1.22E-10	-1.22E-10	6.10E-11	-6.10E-11
CLKIN	0	0	0	0	-1.83E-10
TIN	0	0	-1.83E-10	6.10E-11	6.10E-11
SEL1	-6.10E-11	-1.22E-10	-1.22E-10	-1.22E-10	0
SEL2	-1.83E-10	0	-6.10E-11	0	0
SEL3	0	0	6.10E-11	0	-1.22E-10
SEL4	-6.10E-11	6.10E-11	6.10E-11	-1.22E-10	1.83E-10
Q0	-1.83E-10	-6.10E-11	6.10E-11	-6.10E-11	-6.10E-11
Q1	0	0	-6.10E-11	-1.83E-10	-1.83E-10
Q2	-1.83E-10	-1.22E-10	-1.83E-10	6.10E-11	0
Q3	0	-6.10E-11	6.10E-11	-1.83E-10	-6.10E-11

IIH Params: Vin = VCC, Min = -10UA/Max = 10UA

VCC	4.5	4.75	5	5.25	5.5
RESET	2.44E-10	0	1.22E-10	1.22E-10	0
OE	1.22E-10	1.83E-10	1.22E-10	0	0
LOAD	6.10E-11	1.22E-10	6.10E-11	6.10E-11	1.22E-10
CLKIN	1.83E-10	1.83E-10	6.10E-11	1.22E-10	1.22E-10
TIN	6.10E-11	1.22E-10	6.10E-11	6.10E-11	6.10E-11
SEL1	0	6.10E-11	-6.10E-11	0	1.22E-10
SEL2	1.83E-10	1.22E-10	1.22E-10	1.83E-10	1.22E-10
SEL3	1.83E-10	-6.10E-11	1.83E-10	1.83E-10	3.66E-10
SEL4	6.10E-11	1.83E-10	2.44E-10	1.22E-10	1.83E-10
Q0	1.22E-10	6.10E-11	1.22E-10	6.10E-11	1.83E-10
Q1	6.10E-11	2.44E-10	1.22E-10	1.22E-10	0
Q2	1.83E-10	1.83E-10	1.22E-10	-6.10E-11	1.22E-10
Q3	1.22E-10	2.44E-10	1.22E-10	6.10E-11	1.22E-10

IOZL Params: Vin = 0.00V, Min = -10UA/Max = 10UA

VCC	4.5	4.75	5	5.25	5.5
DCE0	0	0	6.10E-11	-1.83E-10	6.10E-11
DCE1	-6.10E-11	-6.10E-11	0	0	-1.22E-10
DCE2	-6.10E-11	0	6.10E-11	0	-6.10E-11
DCE3	0	-6.10E-11	1.22E-10	1.22E-10	-1.22E-10
DCE4	0	1.22E-10	0	-6.10E-11	-6.10E-11
DCE5	0	0	-6.10E-11	0	0
DCE6	6.10E-11	-6.10E-11	0	-6.10E-11	-2.44E-10
DCE7	-6.10E-11	6.10E-11	6.10E-11	-6.10E-11	-1.22E-10
DCE8	-1.22E-10	0	6.10E-11	6.10E-11	-6.10E-11
DCE9	0	1.22E-10	0	0	6.10E-11
DCE10	0	-6.10E-11	6.10E-11	0	6.10E-11
DCE11	6.10E-11	-6.10E-11	0	0	-6.10E-11
DCE12	0	1.22E-10	0	0	-1.22E-10

DCE13	6.10E-11	-1.22E-10	-6.10E-11	-1.22E-10	0
DCE14	0	0	0	-6.10E-11	0
DCE15	0	1.22E-10	0	0	6.10E-11
DCE16	6.10E-11	0	-6.10E-11	-6.10E-11	0
DCE17	0	0	-1.22E-10	-1.22E-10	-6.10E-11
DCE18	0	-1.83E-10	0	-6.10E-11	-1.22E-10
DCE19	0	-1.22E-10	0	-1.22E-10	-1.83E-10
DCE20	6.10E-11	-2.44E-10	-6.10E-11	-1.83E-10	-6.10E-11
DCE21	-1.83E-10	-1.22E-10	-1.83E-10	1.83E-10	6.10E-11
DCE22	6.10E-11	0	-1.83E-10	0	-1.83E-10
DCE23	-1.22E-10	-6.10E-11	-6.10E-11	6.10E-11	0
DCE24	-6.10E-11	-1.22E-10	6.10E-11	-1.22E-10	-1.22E-10
DCE25	-6.10E-11	0	-6.10E-11	0	0
DCE26	-6.10E-11	-1.83E-10	6.10E-11	-6.10E-11	1.22E-10
DCE27	6.10E-11	0	-6.10E-11	6.10E-11	0
DCE28	0	6.10E-11	-6.10E-11	0	6.10E-11
DCE29	-6.10E-11	0	-1.22E-10	-1.83E-10	0
DCE30	-1.22E-10	-6.10E-11	-6.10E-11	1.22E-10	0
DCE31	1.22E-10	6.10E-11	0	0	0
DCE32	6.10E-11	1.83E-10	1.83E-10	0	-1.83E-10
DCE33	-6.10E-11	1.22E-10	-6.10E-11	-3.66E-10	0
DCE34	-2.44E-10	1.22E-10	6.10E-11	6.10E-11	-1.83E-10
DCE35	0	-1.22E-10	0	-6.10E-11	-6.10E-11
DCE36	6.10E-11	-1.83E-10	1.22E-10	-1.83E-10	-1.22E-10
DCE37	0	6.10E-11	0	0	0
DCE38	0	-6.10E-11	1.22E-10	-1.83E-10	-1.22E-10
DCE39	0	-6.10E-11	-2.44E-10	0	6.10E-11
MOUT40	0	-2.44E-10	0	6.10E-11	0
MOUT41	-1.22E-10	0	-6.10E-11	-1.22E-10	0
MOUT42	-1.83E-10	6.10E-11	0	0	0
MOUT43	0	-1.22E-10	0	-6.10E-11	-6.10E-11
MOUT44	0	0	6.10E-11	6.10E-11	-2.44E-10
MOUT45	-1.83E-10	-1.22E-10	0	1.22E-10	0
MOUT46	-6.10E-11	6.10E-11	6.10E-11	-6.10E-11	0
MOUT47	-6.10E-11		6.10E-11	6.10E-11	

IOZH Params: Vin = VCC, Min = -10UA/Max = 10UA					
VCC	4.5	4.75	5	5.25	5.5
DCE0	1.22E-10	1.83E-10	3.05E-10	3.05E-10	2.44E-10
DCE1	1.83E-10	1.83E-10	1.22E-10	6.10E-11	0
DCE2	1.83E-10	0	1.22E-10	1.22E-10	1.22E-10
DCE3	2.44E-10	6.10E-11	1.22E-10	1.83E-10	1.22E-10
DCE4	-6.10E-11	1.22E-10	2.44E-10	1.22E-10	0
DCE5	1.22E-10	6.10E-11	6.10E-11	1.83E-10	2.44E-10
DCE6	1.22E-10	6.10E-11	2.44E-10	0	1.22E-10
DCE7	-6.10E-11	6.10E-11	6.10E-11	3.05E-10	0
DCE8	6.10E-11	1.83E-10	6.10E-11	3.05E-10	0
DCE9	6.10E-11	6.10E-11	1.83E-10	6.10E-11	1.22E-10
DCE10	1.83E-10	0	6.10E-11	6.10E-11	1.22E-10
DCE11	1.22E-10	6.10E-11	6.10E-11	6.10E-11	2.44E-10
DCE12	0	6.10E-11	1.83E-10	6.10E-11	0
DCE13	1.83E-10	1.22E-10	2.44E-10	1.83E-10	1.22E-10
DCE14	1.83E-10	6.10E-11	1.83E-10	6.10E-11	1.22E-10
DCE15	6.10E-11	3.05E-10	1.22E-10	0	1.22E-10
DCE16	2.44E-10	1.83E-10	3.05E-10	3.05E-10	-1.22E-10
DCE17	6.10E-11	1.22E-10	1.83E-10	0	6.10E-11
DCE18	6.10E-11	6.10E-11	6.10E-11	6.10E-11	1.83E-10
DCE19	1.22E-10	1.83E-10	1.22E-10	0	6.10E-11
DCE20	1.22E-10	6.10E-11	1.83E-10	6.10E-11	1.22E-10
DCE21	0	6.10E-11	0	-1.22E-10	6.10E-11
DCE22	1.22E-10	6.10E-11	1.22E-10	6.10E-11	6.10E-11
DCE23	1.22E-10	-6.10E-11	6.10E-11	6.10E-11	0
DCE24	0	-6.10E-11	0	6.10E-11	6.10E-11
DCE25	2.44E-10	3.05E-10	1.83E-10	0	1.22E-10

DCE26	6.10E-11	1.22E-10	6.10E-11	-6.10E-11	2.44E-10
DCE27	6.10E-11	1.22E-10	2.44E-10	1.22E-10	1.22E-10
DCE28	1.22E-10	1.83E-10	1.22E-10	1.83E-10	1.22E-10
DCE29	1.22E-10	6.10E-11	1.22E-10	6.10E-11	1.22E-10
DCE30	3.05E-10	1.83E-10	-6.10E-11	3.05E-10	1.22E-10
DCE31	1.83E-10	1.22E-10	2.44E-10	1.22E-10	6.10E-11
DCE32	6.10E-11	6.10E-11	1.83E-10	1.83E-10	6.10E-11
DCE33	0	-6.10E-11	0	6.10E-11	0
DCE34	1.22E-10	0	3.05E-10	1.83E-10	2.44E-10
DCE35	6.10E-11	6.10E-11	1.22E-10	0	1.22E-10
DCE36	2.44E-10	6.10E-11	6.10E-11	6.10E-11	0
DCE37	1.83E-10	1.22E-10	-6.10E-11	-6.10E-11	6.10E-11
DCE38	1.22E-10	1.22E-10	1.22E-10	1.83E-10	6.10E-11
DCE39	1.83E-10	-6.10E-11	6.10E-11	6.10E-11	0
MOUT40	6.10E-11	0	1.83E-10	6.10E-11	-6.10E-11
MOUT41	1.83E-10	2.44E-10	-1.22E-10	1.22E-10	1.22E-10
MOUT42	1.83E-10	0	2.44E-10	6.10E-11	1.22E-10
MOUT43	0	6.10E-11	6.10E-11	6.10E-11	1.22E-10
MOUT44	1.83E-10	0	1.22E-10	6.10E-11	1.83E-10
MOUT45	1.83E-10	6.10E-11	6.10E-11	1.22E-10	6.10E-11
MOUT46	-6.10E-11	0	2.44E-10	-6.10E-11	1.22E-10
MOUT47	3.05E-10	0	6.10E-11	6.10E-11	6.10E-11

IOS Params:VO =0.00V, Min=-100mA/Max=-10mA

VCC	4.5	4.75	5	5.25	5.5
Q0	-2.23E-02	-2.47E-02	-2.70E-02	-2.93E-02	-3.18E-02
Q1	-2.23E-02	-2.45E-02	-2.68E-02	-2.92E-02	-3.16E-02
Q2	-2.20E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.13E-02
Q3	-2.19E-02	-2.41E-02	-2.65E-02	-2.88E-02	-3.12E-02
FF1	-2.23E-02	-2.45E-02	-2.68E-02	-2.92E-02	-3.16E-02
FF2	-2.23E-02	-2.46E-02	-2.70E-02	-2.94E-02	-3.18E-02
TOUT1	-2.15E-02	-2.38E-02	-2.60E-02	-2.84E-02	-3.07E-02
TOUT5	-2.17E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE0	-2.17E-02	-2.40E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE1	-2.17E-02	-2.40E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE2	-2.19E-02	-2.41E-02	-2.65E-02	-2.88E-02	-3.12E-02
DCE3	-2.16E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE4	-2.23E-02	-2.46E-02	-2.70E-02	-2.93E-02	-3.18E-02
DCE5	-2.21E-02	-2.45E-02	-2.68E-02	-2.91E-02	-3.15E-02
DCE6	-2.23E-02	-2.46E-02	-2.70E-02	-2.93E-02	-3.17E-02
DCE7	-2.24E-02	-2.48E-02	-2.71E-02	-2.95E-02	-3.20E-02
DCE8	-2.23E-02	-2.46E-02	-2.70E-02	-2.94E-02	-3.18E-02
DCE9	-2.23E-02	-2.46E-02	-2.70E-02	-2.94E-02	-3.18E-02
DCE10	-2.25E-02	-2.48E-02	-2.71E-02	-2.95E-02	-3.20E-02
DCE11	-2.21E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.14E-02
DCE12	-2.19E-02	-2.42E-02	-2.65E-02	-2.89E-02	-3.13E-02
DCE13	-2.20E-02	-2.43E-02	-2.66E-02	-2.89E-02	-3.13E-02
DCE14	-2.21E-02	-2.44E-02	-2.67E-02	-2.90E-02	-3.15E-02
DCE15	-2.20E-02	-2.43E-02	-2.66E-02	-2.89E-02	-3.13E-02
DCE16	-2.17E-02	-2.40E-02	-2.62E-02	-2.86E-02	-3.09E-02
DCE17	-2.16E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE18	-2.17E-02	-2.40E-02	-2.63E-02	-2.86E-02	-3.10E-02
DCE19	-2.19E-02	-2.41E-02	-2.65E-02	-2.88E-02	-3.12E-02
DCE20	-2.15E-02	-2.37E-02	-2.60E-02	-2.84E-02	-3.07E-02
DCE21	-2.16E-02	-2.38E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE22	-2.16E-02	-2.38E-02	-2.62E-02	-2.84E-02	-3.07E-02
DCE23	-2.16E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.08E-02
DCE24	-2.16E-02	-2.38E-02	-2.61E-02	-2.84E-02	-3.07E-02
DCE25	-2.16E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE26	-2.19E-02	-2.41E-02	-2.65E-02	-2.88E-02	-3.12E-02
DCE27	-2.18E-02	-2.41E-02	-2.64E-02	-2.88E-02	-3.12E-02
DCE28	-2.18E-02	-2.41E-02	-2.64E-02	-2.88E-02	-3.12E-02
DCE29	-2.16E-02	-2.39E-02	-2.62E-02	-2.85E-02	-3.09E-02
DCE30	-2.18E-02	-2.41E-02	-2.64E-02	-2.87E-02	-3.11E-02

DCE31	-2.15E-02	-2.37E-02	-2.60E-02	-2.83E-02	-3.06E-02
DCE32	-2.24E-02	-2.47E-02	-2.71E-02	-2.95E-02	-3.19E-02
DCE33	-2.24E-02	-2.47E-02	-2.71E-02	-2.95E-02	-3.18E-02
DCE34	-2.22E-02	-2.45E-02	-2.68E-02	-2.92E-02	-3.16E-02
DCE35	-2.23E-02	-2.46E-02	-2.70E-02	-2.93E-02	-3.17E-02
DCE36	-2.19E-02	-2.41E-02	-2.65E-02	-2.88E-02	-3.12E-02
DCE37	-2.20E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.13E-02
DCE38	-2.20E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.14E-02
DCE39	-2.22E-02	-2.45E-02	-2.68E-02	-2.92E-02	-3.16E-02
MOUT40	-2.16E-02	-2.38E-02	-2.61E-02	-2.84E-02	-3.07E-02
MOUT41	-2.13E-02	-2.35E-02	-2.58E-02	-2.80E-02	-3.04E-02
MOUT42	-2.23E-02	-2.47E-02	-2.70E-02	-2.93E-02	-3.17E-02
MOUT43	-2.21E-02	-2.44E-02	-2.67E-02	-2.91E-02	-3.15E-02
MOUT44	-2.20E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.13E-02
MOUT45	-2.21E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.14E-02
MOUT46	-2.20E-02	-2.43E-02	-2.66E-02	-2.90E-02	-3.14E-02
MOUT47	-2.21E-02	-2.44E-02	-2.68E-02	-2.91E-02	-3.15E-02

IOSP Params:VO = VCC, Min = 20mA/Max = 140mA					
VCC	4.5	4.75	5	5.25	5.5
Q0	5.95E-02	6.43E-02	6.90E-02	7.36E-02	7.81E-02
Q1	5.96E-02	6.43E-02	6.90E-02	7.36E-02	7.80E-02
Q2	5.99E-02	6.46E-02	6.93E-02	7.40E-02	7.85E-02
Q3	5.99E-02	6.46E-02	6.94E-02	7.40E-02	7.85E-02
FF1	5.95E-02	6.43E-02	6.89E-02	7.35E-02	7.80E-02
FF2	5.96E-02	6.44E-02	6.91E-02	7.37E-02	7.82E-02
TOUT1	5.95E-02	6.42E-02	6.88E-02	7.34E-02	7.78E-02
TOUT5	5.91E-02	6.38E-02	6.84E-02	7.29E-02	7.73E-02
DCE0	6.00E-02	6.49E-02	6.96E-02	7.43E-02	7.88E-02
DCE1	6.01E-02	6.49E-02	6.96E-02	7.43E-02	7.88E-02
DCE2	5.98E-02	6.45E-02	6.93E-02	7.39E-02	7.85E-02
DCE3	5.95E-02	6.43E-02	6.90E-02	7.37E-02	7.82E-02
DCE4	5.89E-02	6.37E-02	6.83E-02	7.29E-02	7.73E-02
DCE5	5.92E-02	6.39E-02	6.85E-02	7.31E-02	7.76E-02
DCE6	5.92E-02	6.39E-02	6.85E-02	7.32E-02	7.76E-02
DCE7	5.91E-02	6.39E-02	6.85E-02	7.31E-02	7.76E-02
DCE8	5.95E-02	6.43E-02	6.90E-02	7.37E-02	7.82E-02
DCE9	5.96E-02	6.43E-02	6.90E-02	7.37E-02	7.82E-02
DCE10	5.98E-02	6.46E-02	6.93E-02	7.40E-02	7.85E-02
DCE11	6.02E-02	6.51E-02	6.98E-02	7.45E-02	7.90E-02
DCE12	6.01E-02	6.49E-02	6.96E-02	7.43E-02	7.88E-02
DCE13	5.98E-02	6.46E-02	6.93E-02	7.39E-02	7.85E-02
DCE14	5.96E-02	6.44E-02	6.90E-02	7.37E-02	7.82E-02
DCE15	5.96E-02	6.43E-02	6.90E-02	7.37E-02	7.82E-02
DCE16	5.95E-02	6.43E-02	6.90E-02	7.35E-02	7.81E-02
DCE17	5.92E-02	6.40E-02	6.87E-02	7.33E-02	7.79E-02
DCE18	5.90E-02	6.37E-02	6.84E-02	7.30E-02	7.75E-02
DCE19	5.91E-02	6.38E-02	6.84E-02	7.30E-02	7.76E-02
DCE20	5.84E-02	6.30E-02	6.76E-02	7.20E-02	7.64E-02
DCE21	5.85E-02	6.32E-02	6.77E-02	7.23E-02	7.66E-02
DCE22	5.85E-02	6.32E-02	6.78E-02	7.23E-02	7.66E-02
DCE23	5.86E-02	6.33E-02	6.79E-02	7.24E-02	7.68E-02
DCE24	5.87E-02	6.34E-02	6.80E-02	7.25E-02	7.69E-02
DCE25	5.85E-02	6.32E-02	6.78E-02	7.23E-02	7.67E-02
DCE26	5.83E-02	6.29E-02	6.75E-02	7.19E-02	7.63E-02
DCE27	5.84E-02	6.30E-02	6.76E-02	7.21E-02	7.65E-02
DCE28	5.84E-02	6.30E-02	6.76E-02	7.20E-02	7.63E-02
DCE29	5.82E-02	6.29E-02	6.74E-02	7.19E-02	7.63E-02
DCE30	5.82E-02	6.28E-02	6.73E-02	7.18E-02	7.61E-02
DCE31	5.80E-02	6.26E-02	6.71E-02	7.15E-02	7.59E-02
DCE32	5.94E-02	6.41E-02	6.88E-02	7.34E-02	7.79E-02
DCE33	5.95E-02	6.42E-02	6.89E-02	7.35E-02	7.80E-02
DCE34	5.99E-02	6.48E-02	6.95E-02	7.41E-02	7.87E-02
DCE35	6.00E-02	6.48E-02	6.95E-02	7.41E-02	7.87E-02

DCE36	5.98E-02	6.46E-02	6.93E-02	7.40E-02	7.85E-02
DCE37	5.91E-02	6.38E-02	6.85E-02	7.30E-02	7.76E-02
DCE38	5.91E-02	6.38E-02	6.84E-02	7.30E-02	7.76E-02
DCE39	5.88E-02	6.35E-02	6.82E-02	7.27E-02	7.72E-02
MOUT40	5.87E-02	6.34E-02	6.80E-02	7.25E-02	7.69E-02
MOUT41	5.90E-02	6.38E-02	6.84E-02	7.29E-02	7.73E-02
MOUT42	5.91E-02	6.38E-02	6.84E-02	7.30E-02	7.74E-02
MOUT43	5.92E-02	6.39E-02	6.85E-02	7.31E-02	7.76E-02
MOUT44	5.92E-02	6.39E-02	6.85E-02	7.31E-02	7.75E-02
MOUT45	5.96E-02	6.44E-02	6.91E-02	7.38E-02	7.83E-02
MOUT46	5.96E-02	6.44E-02	6.91E-02	7.37E-02	7.83E-02
MOUT47	5.96E-02	6.44E-02	6.91E-02	7.38E-02	7.83E-02

VIH Params: Max = 2.0V/Min = 0.8V

VCC	4.5	4.75	5	5.25	5.5
RESET	1.3301	1.3711	1.4199	1.4688	1.5215
OE	1.3203	1.3711	1.4199	1.4688	1.4961
LOAD	1.3242	1.3652	1.418	1.4844	1.498
CLKIN	1.3613	1.4277	1.4902	1.5547	1.6172
TIN	1.3379	1.3926	1.4355	1.4805	1.5352
SEL1	1.3184	1.3691	1.418	1.4648	1.5098
SEL2	1.3125	1.3633	1.4121	1.459	1.5078
SEL3	1.3242	1.377	1.4258	1.4707	1.5137
SEL4	1.3047	1.3555	1.4043	1.4551	1.502
Q0	1.3008	1.3516	1.4023	1.4492	1.4961
Q1	1.3086	1.3555	1.4043	1.4512	1.498
Q2	1.3027	1.3516	1.3984	1.4453	1.4902
Q3	1.3027	1.3516	1.4004	1.4512	1.4941

VIL Params: Max = 2.0V/Min = 0.8V

VCC	4.5	4.75	5	5.25	5.5
RESET	1.291	1.3379	1.3848	1.4316	1.4766
OE	1.2344	1.2598	1.3086	1.3535	1.4004
LOAD	1.2676	1.3086	1.3574	1.4043	1.4492
CLKIN	1.0723	1.1152	1.1582	1.2012	1.2422
TIN	1.1895	1.2324	1.2813	1.3281	1.375
SEL1	1.1523	1.1895	1.2383	1.2852	1.332
SEL2	1.1602	1.1895	1.2324	1.2754	1.3164
SEL3	1.1602	1.1953	1.2422	1.291	1.334
SEL4	1.1484	1.1914	1.2461	1.2969	1.3457
Q0	1.2324	1.2813	1.3281	1.375	1.4199
Q1	1.2676	1.3184	1.3633	1.4102	1.457
Q2	1.2148	1.2637	1.3105	1.3574	1.4023
Q3	1.2168	1.2656	1.3145	1.3594	1.4043

DEVICE PASSED ALL TESTS

JPL Alpha-11 A1020 FPGA Temp: 25 Ser #: 10
03-APR-1992 11:57:25.21 Datecode: 9129 Page: 1
Source file: alpha11.C:H35
Endpoint: 2000hrs

Tpzl Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	LIMIT @ 5V only
DCE0	7.05E-08	6.88E-08	6.54E-08	6.32E-08	6.15E-08	1.5E-07
DCE1	7.17E-08	6.95E-08	6.63E-08	6.46E-08	6.27E-08	1.5E-07
DCE2	6.92E-08	6.72E-08	6.39E-08	6.19E-08	6.01E-08	1.5E-07
DCE3	7.03E-08	6.68E-08	6.45E-08	6.26E-08	6.09E-08	1.5E-07
DCE4	6.82E-08	6.49E-08	6.27E-08	6.05E-08	5.89E-08	1.5E-07
DCE5	6.77E-08	6.59E-08	6.28E-08	6.05E-08	5.87E-08	1.5E-07
DCE6	6.78E-08	6.53E-08	6.23E-08	6.04E-08	5.86E-08	1.5E-07
DCE7	6.77E-08	6.44E-08	6.21E-08	6.01E-08	5.84E-08	1.5E-07
DCE8	6.71E-08	6.58E-08	6.27E-08	5.97E-08	5.86E-08	1.5E-07
DCE9	6.67E-08	6.50E-08	6.23E-08	5.97E-08	5.82E-08	1.5E-07
DCE10	6.66E-08	6.47E-08	6.13E-08	5.93E-08	5.77E-08	1.5E-07
DCE11	6.68E-08	6.38E-08	6.16E-08	5.96E-08	5.79E-08	1.5E-07
DCE12	6.70E-08	6.40E-08	6.16E-08	5.98E-08	5.81E-08	1.5E-07
DCE13	6.67E-08	6.49E-08	6.17E-08	5.96E-08	5.79E-08	1.5E-07
DCE14	6.69E-08	6.48E-08	6.17E-08	5.96E-08	5.80E-08	1.5E-07
DCE15	6.69E-08	6.38E-08	6.16E-08	5.95E-08	5.79E-08	1.5E-07
DCE16	4.95E-08	4.84E-08	4.69E-08	4.55E-08	4.47E-08	1.5E-07
DCE17	5.07E-08	4.99E-08	4.80E-08	4.73E-08	4.63E-08	1.5E-07
DCE18	5.44E-08	5.36E-08	5.17E-08	5.08E-08	5.00E-08	1.5E-07
DCE19	5.58E-08	5.44E-08	5.32E-08	5.22E-08	5.13E-08	1.5E-07
DCE20	5.97E-08	5.80E-08	5.67E-08	5.55E-08	5.46E-08	1.5E-07
DCE21	5.98E-08	5.89E-08	5.70E-08	5.58E-08	5.48E-08	1.5E-07
DCE22	5.98E-08	5.89E-08	5.70E-08	5.58E-08	5.47E-08	1.5E-07
DCE23	5.97E-08	5.81E-08	5.67E-08	5.56E-08	5.47E-08	1.5E-07
DCE24	5.64E-08	5.46E-08	5.18E-08	4.94E-08	4.75E-08	1.5E-07
DCE25	5.57E-08	5.38E-08	5.14E-08	4.90E-08	4.69E-08	1.5E-07
DCE26	5.59E-08	5.39E-08	5.08E-08	4.87E-08	4.70E-08	1.5E-07
DCE27	5.59E-08	5.30E-08	5.06E-08	4.86E-08	4.70E-08	1.5E-07
DCE28	5.61E-08	5.33E-08	5.09E-08	4.88E-08	4.71E-08	1.5E-07
DCE29	5.55E-08	5.28E-08	5.03E-08	4.85E-08	4.68E-08	1.5E-07
DCE30	5.61E-08	5.33E-08	5.09E-08	4.89E-08	4.72E-08	1.5E-07
DCE31	5.56E-08	5.29E-08	5.05E-08	4.84E-08	4.67E-08	1.5E-07
DCE32	6.29E-08	6.21E-08	6.03E-08	5.90E-08	5.80E-08	1.5E-07
DCE33	6.26E-08	6.16E-08	5.94E-08	5.84E-08	5.74E-08	1.5E-07
DCE34	6.54E-08	6.43E-08	6.24E-08	6.13E-08	6.05E-08	1.5E-07
DCE35	5.98E-08	5.82E-08	5.69E-08	5.59E-08	5.49E-08	1.5E-07
DCE36	6.18E-08	6.01E-08	5.88E-08	5.78E-08	5.70E-08	1.5E-07
DCE37	5.82E-08	5.64E-08	5.53E-08	5.43E-08	5.34E-08	1.5E-07
DCE38	6.04E-08	5.86E-08	5.74E-08	5.64E-08	5.53E-08	1.5E-07
DCE39	6.62E-08	6.45E-08	6.32E-08	6.20E-08	6.10E-08	1.5E-07
MOUT40	8.63E-08	8.49E-08	8.04E-08	7.79E-08	7.55E-08	1.5E-07
MOUT41	8.66E-08	8.49E-08	8.04E-08	7.79E-08	7.55E-08	1.5E-07
MOUT42	8.83E-08	8.62E-08	8.18E-08	7.93E-08	7.72E-08	1.5E-07
MOUT43	8.23E-08	8.11E-08	7.67E-08	7.44E-08	7.25E-08	1.5E-07
MOUT44	8.14E-08	7.89E-08	7.46E-08	7.23E-08	7.03E-08	1.5E-07
MOUT45	7.89E-08	7.72E-08	7.26E-08	7.04E-08	6.85E-08	1.5E-07
MOUT46	7.67E-08	7.49E-08	7.06E-08	6.84E-08	6.65E-08	1.5E-07

MOUT47	7.82E-08	7.64E-08	7.19E-08	6.96E-08	6.77E-08	1.5E-07

Tpzh Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	LIMIT
DCE0	8.02E-08	7.48E-08	7.02E-08	6.64E-08	6.41E-08	1.5E-07
DCE1	8.24E-08	7.67E-08	7.20E-08	6.88E-08	6.62E-08	1.5E-07
DCE2	8.01E-08	7.63E-08	7.02E-08	6.71E-08	6.42E-08	1.5E-07
DCE3	8.12E-08	7.67E-08	7.11E-08	6.77E-08	6.54E-08	1.5E-07
DCE4	7.90E-08	7.46E-08	6.88E-08	6.54E-08	6.31E-08	1.5E-07
DCE5	7.89E-08	7.50E-08	6.88E-08	6.55E-08	6.31E-08	1.5E-07
DCE6	7.89E-08	7.47E-08	6.88E-08	6.54E-08	6.28E-08	1.5E-07
DCE7	7.87E-08	7.47E-08	6.88E-08	6.54E-08	6.31E-08	1.5E-07
DCE8	7.63E-08	7.34E-08	6.73E-08	6.41E-08	6.23E-08	1.5E-07
DCE9	7.79E-08	7.38E-08	6.85E-08	6.42E-08	6.23E-08	1.5E-07
DCE10	7.75E-08	7.36E-08	6.85E-08	6.42E-08	6.21E-08	1.5E-07
DCE11	7.79E-08	7.39E-08	6.88E-08	6.42E-08	6.25E-08	1.5E-07
DCE12	7.82E-08	7.43E-08	6.88E-08	6.51E-08	6.25E-08	1.5E-07
DCE13	7.79E-08	7.40E-08	6.88E-08	6.42E-08	6.22E-08	1.5E-07
DCE14	7.81E-08	7.41E-08	6.88E-08	6.42E-08	6.25E-08	1.5E-07
DCE15	7.81E-08	7.41E-08	6.88E-08	6.42E-08	6.24E-08	1.5E-07
DCE16	5.89E-08	5.67E-08	5.07E-08	4.87E-08	4.74E-08	1.5E-07
DCE17	6.09E-08	5.84E-08	5.20E-08	5.01E-08	4.84E-08	1.5E-07
DCE18	6.42E-08	6.26E-08	5.71E-08	5.46E-08	5.30E-08	1.5E-07
DCE19	6.62E-08	6.39E-08	5.74E-08	5.58E-08	5.41E-08	1.5E-07
DCE20	7.11E-08	6.86E-08	6.62E-08	5.97E-08	5.84E-08	1.5E-07
DCE21	7.08E-08	6.84E-08	6.34E-08	5.97E-08	5.82E-08	1.5E-07
DCE22	7.12E-08	6.86E-08	6.62E-08	5.97E-08	5.86E-08	1.5E-07
DCE23	7.11E-08	6.86E-08	6.41E-08	5.97E-08	5.85E-08	1.5E-07
DCE24	6.61E-08	6.27E-08	5.67E-08	5.31E-08	5.07E-08	1.5E-07
DCE25	6.73E-08	6.34E-08	5.64E-08	5.32E-08	5.07E-08	1.5E-07
DCE26	6.75E-08	6.37E-08	5.69E-08	5.34E-08	5.09E-08	1.5E-07
DCE27	6.74E-08	6.37E-08	5.68E-08	5.32E-08	5.08E-08	1.5E-07
DCE28	6.73E-08	6.37E-08	5.69E-08	5.34E-08	5.07E-08	1.5E-07
DCE29	6.71E-08	6.34E-08	5.63E-08	5.29E-08	5.05E-08	1.5E-07
DCE30	6.75E-08	6.37E-08	5.67E-08	5.34E-08	5.09E-08	1.5E-07
DCE31	6.75E-08	6.37E-08	5.68E-08	5.32E-08	5.07E-08	1.5E-07
DCE32	7.21E-08	7.03E-08	6.57E-08	6.28E-08	6.12E-08	1.5E-07
DCE33	7.30E-08	7.05E-08	6.62E-08	6.31E-08	6.13E-08	1.5E-07
DCE34	8.13E-08	7.78E-08	7.38E-08	6.98E-08	6.78E-08	1.5E-07
DCE35	7.06E-08	6.42E-08	6.15E-08	5.96E-08	5.80E-08	1.5E-07
DCE36	7.26E-08	7.03E-08	6.81E-08	6.30E-08	6.10E-08	1.5E-07
DCE37	6.88E-08	6.64E-08	6.14E-08	5.86E-08	5.69E-08	1.5E-07
DCE38	7.11E-08	6.87E-08	6.32E-08	5.97E-08	5.86E-08	1.5E-07
DCE39	7.71E-08	7.44E-08	6.88E-08	6.68E-08	6.49E-08	1.5E-07
MOUT40	8.90E-08	8.42E-08	8.11E-08	7.86E-08	7.64E-08	1.5E-07
MOUT41	8.95E-08	8.46E-08	8.13E-08	7.87E-08	7.65E-08	1.5E-07
MOUT42	8.85E-08	8.50E-08	8.20E-08	7.94E-08	7.73E-08	1.5E-07
MOUT43	8.49E-08	8.08E-08	7.77E-08	7.52E-08	7.32E-08	1.5E-07
MOUT44	8.30E-08	7.87E-08	7.56E-08	7.31E-08	7.11E-08	1.5E-07
MOUT45	8.18E-08	7.71E-08	7.38E-08	7.13E-08	6.92E-08	1.5E-07
MOUT46	7.93E-08	7.49E-08	7.19E-08	6.93E-08	6.72E-08	1.5E-07
MOUT47	8.16E-08	7.63E-08	7.31E-08	7.06E-08	6.86E-08	1.5E-07

Tplz Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	LIMIT
DCE0	7.57E-08	6.97E-08	6.91E-08	6.83E-08	6.78E-08	1.5E-07
DCE1	7.07E-08	6.91E-08	6.84E-08	6.75E-08	6.68E-08	1.5E-07
DCE2	7.10E-08	6.92E-08	6.85E-08	6.78E-08	6.72E-08	1.5E-07
DCE3	7.39E-08	6.80E-08	6.72E-08	6.66E-08	6.59E-08	1.5E-07
DCE4	7.41E-08	6.82E-08	6.72E-08	6.64E-08	6.60E-08	1.5E-07
DCE5	7.33E-08	6.82E-08	6.63E-08	6.55E-08	6.48E-08	1.5E-07
DCE6	7.41E-08	7.34E-08	7.23E-08	7.13E-08	7.02E-08	1.5E-07
DCE7	7.39E-08	7.29E-08	7.18E-08	6.66E-08	6.99E-08	1.5E-07
DCE8	7.08E-08	6.64E-08	6.84E-08	6.37E-08	6.29E-08	1.5E-07
DCE9	7.19E-08	7.04E-08	6.96E-08	6.88E-08	6.82E-08	1.5E-07
DCE10	7.16E-08	7.03E-08	6.95E-08	6.87E-08	6.82E-08	1.5E-07
DCE11	7.17E-08	7.04E-08	6.96E-08	6.88E-08	6.83E-08	1.5E-07
DCE12	7.11E-08	7.01E-08	6.93E-08	6.79E-08	6.73E-08	1.5E-07
DCE13	7.08E-08	6.99E-08	6.55E-08	6.50E-08	6.42E-08	1.5E-07
DCE14	7.13E-08	7.04E-08	6.92E-08	6.84E-08	6.77E-08	1.5E-07
DCE15	7.13E-08	6.97E-08	6.88E-08	6.81E-08	6.75E-08	1.5E-07
DCE16	7.17E-08	7.09E-08	6.65E-08	6.89E-08	6.84E-08	1.5E-07
DCE17	7.00E-08	6.93E-08	6.86E-08	6.32E-08	6.21E-08	1.5E-07
DCE18	7.35E-08	7.25E-08	7.08E-08	6.94E-08	6.88E-08	1.5E-07
DCE19	7.68E-08	7.59E-08	7.50E-08	7.37E-08	7.32E-08	1.5E-07
DCE20	8.05E-08	7.97E-08	7.88E-08	7.76E-08	7.69E-08	1.5E-07
DCE21	8.02E-08	7.95E-08	7.86E-08	7.21E-08	7.13E-08	1.5E-07
DCE22	8.06E-08	7.97E-08	7.83E-08	7.76E-08	7.68E-08	1.5E-07
DCE23	8.13E-08	8.03E-08	7.95E-08	7.84E-08	7.76E-08	1.5E-07
DCE24	6.01E-08	5.93E-08	5.80E-08	5.74E-08	5.68E-08	1.5E-07
DCE25	5.99E-08	5.86E-08	5.78E-08	5.70E-08	5.08E-08	1.5E-07
DCE26	6.02E-08	5.90E-08	5.82E-08	5.75E-08	5.64E-08	1.5E-07
DCE27	5.70E-08	5.82E-08	5.74E-08	5.68E-08	4.96E-08	1.5E-07
DCE28	5.95E-08	5.83E-08	5.74E-08	5.67E-08	5.09E-08	1.5E-07
DCE29	5.95E-08	5.82E-08	5.74E-08	5.67E-08	5.60E-08	1.5E-07
DCE30	5.97E-08	5.88E-08	5.74E-08	5.69E-08	5.62E-08	1.5E-07
DCE31	5.91E-08	5.83E-08	5.70E-08	5.11E-08	5.05E-08	1.5E-07
DCE32	9.00E-08	8.93E-08	8.80E-08	8.72E-08	8.65E-08	1.5E-07
DCE33	9.00E-08	8.93E-08	8.84E-08	8.71E-08	8.64E-08	1.5E-07
DCE34	1.02E-07	1.01E-07	9.89E-08	9.84E-08	9.75E-08	1.5E-07
DCE35	8.72E-08	8.64E-08	8.56E-08	8.43E-08	8.37E-08	1.5E-07
DCE36	8.54E-08	8.45E-08	8.29E-08	8.22E-08	8.14E-08	1.5E-07
DCE37	8.49E-08	8.42E-08	8.34E-08	8.27E-08	8.15E-08	1.5E-07
DCE38	7.84E-08	7.76E-08	7.67E-08	7.52E-08	7.45E-08	1.5E-07
DCE39	8.95E-08	8.86E-08	8.76E-08	8.02E-08	8.53E-08	1.5E-07
MOUT40	9.54E-08	9.44E-08	9.26E-08	8.83E-08	9.06E-08	1.5E-07
MOUT41	9.58E-08	9.49E-08	9.38E-08	9.23E-08	9.15E-08	1.5E-07
MOUT42	9.58E-08	9.48E-08	9.36E-08	8.77E-08	8.66E-08	1.5E-07
MOUT43	9.00E-08	8.91E-08	8.83E-08	8.69E-08	8.61E-08	1.5E-07
MOUT44	9.13E-08	9.04E-08	8.95E-08	8.37E-08	8.30E-08	1.5E-07
MOUT45	8.60E-08	8.51E-08	8.36E-08	7.86E-08	8.18E-08	1.5E-07
MOUT46	8.78E-08	8.69E-08	8.61E-08	8.52E-08	7.89E-08	1.5E-07
MOUT47	8.53E-08	8.37E-08	8.28E-08	8.18E-08	8.11E-08	1.5E-07

Tphz Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	LIMIT
DCE0	6.90E-08	6.77E-08	6.66E-08	6.58E-08	6.47E-08	1.5E-07
DCE1	6.88E-08	6.74E-08	6.63E-08	6.53E-08	6.43E-08	1.5E-07
DCE2	6.88E-08	6.74E-08	6.63E-08	6.53E-08	6.44E-08	1.5E-07
DCE3	6.74E-08	6.63E-08	6.53E-08	6.42E-08	6.33E-08	1.5E-07
DCE4	6.75E-08	6.63E-08	6.51E-08	6.41E-08	6.32E-08	1.5E-07
DCE5	6.75E-08	6.62E-08	6.51E-08	6.39E-08	6.28E-08	1.5E-07
DCE6	6.77E-08	6.63E-08	6.51E-08	6.40E-08	6.32E-08	1.5E-07
DCE7	6.75E-08	6.63E-08	6.49E-08	6.37E-08	6.30E-08	1.5E-07
DCE8	6.54E-08	6.41E-08	6.31E-08	6.20E-08	6.10E-08	1.5E-07
DCE9	6.53E-08	6.37E-08	6.26E-08	6.16E-08	6.06E-08	1.5E-07
DCE10	6.49E-08	6.36E-08	6.25E-08	6.14E-08	6.04E-08	1.5E-07
DCE11	6.48E-08	6.35E-08	6.25E-08	6.12E-08	6.04E-08	1.5E-07
DCE12	6.48E-08	6.35E-08	6.25E-08	6.14E-08	6.04E-08	1.5E-07
DCE13	6.48E-08	6.35E-08	6.25E-08	6.13E-08	6.04E-08	1.5E-07
DCE14	6.49E-08	6.35E-08	6.25E-08	6.14E-08	6.05E-08	1.5E-07
DCE15	6.53E-08	6.37E-08	6.27E-08	6.15E-08	6.05E-08	1.5E-07
DCE16	6.52E-08	6.41E-08	6.30E-08	6.20E-08	6.11E-08	1.5E-07
DCE17	6.43E-08	6.32E-08	6.18E-08	6.07E-08	6.00E-08	1.5E-07
DCE18	7.11E-08	6.96E-08	6.86E-08	6.74E-08	6.67E-08	1.5E-07
DCE19	7.00E-08	6.88E-08	6.75E-08	6.64E-08	6.57E-08	1.5E-07
DCE20	7.43E-08	7.28E-08	7.16E-08	7.05E-08	6.93E-08	1.5E-07
DCE21	7.42E-08	7.28E-08	7.16E-08	7.04E-08	6.95E-08	1.5E-07
DCE22	7.44E-08	7.30E-08	7.17E-08	7.06E-08	6.95E-08	1.5E-07
DCE23	7.43E-08	7.30E-08	7.17E-08	7.06E-08	6.95E-08	1.5E-07
DCE24	5.26E-08	5.13E-08	5.03E-08	4.92E-08	4.81E-08	1.5E-07
DCE25	5.26E-08	5.11E-08	5.00E-08	4.89E-08	4.79E-08	1.5E-07
DCE26	5.27E-08	5.16E-08	5.05E-08	4.95E-08	4.84E-08	1.5E-07
DCE27	5.27E-08	5.16E-08	5.05E-08	4.93E-08	4.84E-08	1.5E-07
DCE28	5.27E-08	5.14E-08	5.02E-08	4.90E-08	4.83E-08	1.5E-07
DCE29	5.24E-08	5.11E-08	4.99E-08	4.89E-08	4.79E-08	1.5E-07
DCE30	5.28E-08	5.16E-08	5.04E-08	4.93E-08	4.84E-08	1.5E-07
DCE31	5.25E-08	5.11E-08	4.98E-08	4.88E-08	4.80E-08	1.5E-07
DCE32	8.45E-08	8.31E-08	8.18E-08	8.05E-08	7.95E-08	1.5E-07
DCE33	8.43E-08	8.29E-08	8.15E-08	8.02E-08	7.94E-08	1.5E-07
DCE34	8.85E-08	8.78E-08	8.64E-08	8.39E-08	8.25E-08	1.5E-07
DCE35	8.01E-08	7.90E-08	7.75E-08	7.65E-08	7.58E-08	1.5E-07
DCE36	7.85E-08	7.73E-08	7.59E-08	7.51E-08	7.38E-08	1.5E-07
DCE37	7.84E-08	7.73E-08	7.60E-08	7.51E-08	7.41E-08	1.5E-07
DCE38	7.73E-08	7.58E-08	7.43E-08	7.33E-08	7.23E-08	1.5E-07
DCE39	8.43E-08	8.27E-08	8.12E-08	8.01E-08	7.90E-08	1.5E-07
MOUT40	8.92E-08	8.77E-08	8.62E-08	8.51E-08	8.39E-08	1.5E-07
MOUT41	8.93E-08	8.77E-08	8.63E-08	8.50E-08	8.40E-08	1.5E-07
MOUT42	9.07E-08	8.91E-08	8.77E-08	8.62E-08	8.52E-08	1.5E-07
MOUT43	8.45E-08	8.31E-08	8.18E-08	8.07E-08	7.95E-08	1.5E-07
MOUT44	8.69E-08	8.55E-08	8.42E-08	8.28E-08	8.18E-08	1.5E-07
MOUT45	8.07E-08	7.91E-08	7.78E-08	7.67E-08	7.57E-08	1.5E-07
MOUT46	8.33E-08	8.20E-08	8.05E-08	7.93E-08	7.83E-08	1.5E-07
MOUT47	8.07E-08	7.93E-08	7.80E-08	7.68E-08	7.57E-08	1.5E-07

DEVICE PASSED ALL TESTS

JPL Alpha-11 A1020 FPGA Temp: 25 Ser #: 10
03-APR-1992 10:12:56.90 Datecode: 9129 Page: 1
Source file: alpha11.C:H35
End point: 2000 hrs

Tplh_clk Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	LIMIT VALID @ 5V only
Q0	2.73E-08 *	2.59E-08	2.50E-08	2.41E-08	2.34E-08	**2.68E-08**
Q1	2.80E-08 *	2.67E-08 *	2.55E-08	2.47E-08	2.39E-08	**2.66E-08**
Q2	4.95E-08	4.82E-08	4.71E-08	4.62E-08	4.54E-08	**5.27E-08**
Q3	6.32E-08	6.15E-08	6.01E-08	5.90E-08	5.81E-08	**6.94E-08**
FF1	2.32E-08	2.23E-08	2.16E-08	2.08E-08	2.03E-08	**2.36E-08**
FF2	2.85E-08 *	2.74E-08 *	2.64E-08 *	2.56E-08 *	2.48E-08 *	**2.37E-08**
TOUT1	4.59E-08	4.43E-08	4.31E-08	4.21E-08	4.12E-08	**5.45E-08**
TOUT5	8.66E-08	8.37E-08	8.12E-08	7.90E-08	7.71E-08	**1.07E-07**
DCE0	8.20E-08	7.89E-08	7.64E-08	7.43E-08	7.26E-08	**8.66E-08**
DCE1	7.64E-08	7.49E-08	7.38E-08	7.29E-08	7.20E-08	**8.73E-08**
DCE2	7.21E-08	6.96E-08	6.73E-08	6.55E-08	6.40E-08	**8.65E-08**
DCE3	7.87E-08	7.70E-08	7.56E-08	7.43E-08	7.31E-08	**8.67E-08**
DCE4	8.50E-08	8.22E-08	7.95E-08	7.73E-08	7.55E-08	**8.60E-08**
DCE5	7.56E-08	7.42E-08	7.32E-08	7.24E-08	7.16E-08	**8.67E-08**
DCE6	7.55E-08	7.42E-08	7.31E-08	7.23E-08	7.16E-08	**8.68E-08**
DCE7	8.90E-08 *	8.58E-08	8.30E-08	8.08E-08	7.89E-08	**8.64E-08**
DCE8	5.67E-08	5.48E-08	5.34E-08	5.21E-08	5.09E-08	**6.24E-08**
DCE9	5.57E-08	5.39E-08	5.24E-08	5.11E-08	5.00E-08	**6.07E-08**
DCE10	5.58E-08	5.40E-08	5.25E-08	5.13E-08	5.01E-08	**6.01E-08**
DCE11	5.62E-08	5.44E-08	5.30E-08	5.17E-08	5.07E-08	**6.13E-08**
DCE12	5.45E-08	5.27E-08	5.11E-08	4.98E-08	4.86E-08	**5.97E-08**
DCE13	5.79E-08	5.58E-08	5.41E-08	5.27E-08	5.15E-08	**6.10E-08**
DCE14	5.63E-08	5.44E-08	5.30E-08	5.16E-08	5.05E-08	**6.26E-08**
DCE15	6.18E-08	5.97E-08	5.81E-08	5.66E-08	5.53E-08	**6.36E-08**
DCE16	6.04E-08	5.81E-08	5.61E-08	5.44E-08	5.31E-08	**6.44E-08**
DCE17	6.11E-08	5.88E-08	5.69E-08	5.52E-08	5.39E-08	**6.57E-08**
DCE18	5.95E-08	5.77E-08	5.61E-08	5.49E-08	5.39E-08	**6.41E-08**
DCE19	6.23E-08	6.01E-08	5.81E-08	5.64E-08	5.50E-08	**6.29E-08**
DCE20	6.38E-08	6.11E-08	5.89E-08	5.71E-08	5.56E-08	**6.41E-08**
DCE21	6.03E-08	5.81E-08	5.62E-08	5.47E-08	5.34E-08	**6.45E-08**
DCE22	6.12E-08	5.92E-08	5.76E-08	5.62E-08	5.51E-08	**6.51E-08**
DCE23	6.43E-08	6.22E-08	6.02E-08	5.88E-08	5.75E-08	**6.74E-08**
DCE24	5.88E-08 *	5.65E-08	5.44E-08	5.27E-08	5.11E-08	**5.70E-08**
DCE25	5.36E-08	5.16E-08	4.97E-08	4.82E-08	4.70E-08	**5.57E-08**
DCE26	5.77E-08 *	5.53E-08	5.34E-08	5.17E-08	5.02E-08	**5.63E-08**
DCE27	5.32E-08	5.10E-08	4.92E-08	4.77E-08	4.64E-08	**5.60E-08**
DCE28	5.85E-08 *	5.61E-08 *	5.41E-08	5.23E-08	5.08E-08	**5.50E-08**
DCE29	5.30E-08	5.08E-08	4.91E-08	4.75E-08	4.63E-08	**5.58E-08**
DCE30	5.58E-08 *	5.34E-08	5.16E-08	4.98E-08	4.83E-08	**5.56E-08**
DCE31	5.61E-08	5.39E-08	5.21E-08	5.05E-08	4.91E-08	**6.16E-08**
DCE32	7.01E-08	6.79E-08	6.59E-08	6.44E-08	6.30E-08	**7.54E-08**
DCE33	6.79E-08	6.52E-08	6.30E-08	6.09E-08	5.92E-08	**6.86E-08**
DCE34	7.56E-08 *	7.31E-08 *	7.06E-08 *	6.85E-08	6.66E-08	**7.02E-08**
DCE35	6.83E-08	6.55E-08	6.32E-08	6.12E-08	5.94E-08	**6.91E-08**
DCE36	7.05E-08	6.79E-08	6.57E-08	6.38E-08	6.22E-08	**7.27E-08**
DCE37	6.48E-08 *	6.19E-08	5.96E-08	5.76E-08	5.59E-08	**6.30E-08**
DCE38	6.29E-08	6.05E-08	5.85E-08	5.68E-08	5.54E-08	**6.31E-08**

DCE39	6.51E-08	6.21E-08	5.98E-08	5.77E-08	5.61E-08	**6.60E-08**
MOUT40	8.02E-08	7.71E-08	7.45E-08	7.22E-08	7.06E-08	**8.40E-08**
MOUT41	8.68E-08	8.41E-08	8.19E-08	7.99E-08	7.83E-08	**9.10E-08**
MOUT42	8.72E-08	8.42E-08	8.16E-08	7.94E-08	7.75E-08	**9.67E-08**
MOUT43	9.22E-08	8.93E-08	8.69E-08	8.47E-08	8.30E-08	**1.00E-07**
MOUT44	8.86E-08	8.62E-08	8.42E-08	8.24E-08	8.10E-08	**9.85E-08**
MOUT45	8.56E-08	8.32E-08	8.13E-08	7.96E-08	7.82E-08	**9.22E-08**
MOUT46	7.85E-08	7.60E-08	7.39E-08	7.20E-08	7.05E-08	**8.92E-08**
MOUT47	8.68E-08	8.43E-08	8.18E-08	7.99E-08	7.83E-08	**9.00E-08**

Tphl_clk Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
Q0	2.53E-08	2.46E-08	2.39E-08	2.33E-08	2.29E-08	**2.68E-08**
Q1	2.49E-08	2.40E-08	2.34E-08	2.27E-08	2.23E-08	**2.66E-08**
Q2	4.89E-08	4.80E-08	4.71E-08	4.65E-08	4.57E-08	**5.27E-08**
Q3	6.28E-08	6.18E-08	6.09E-08	6.02E-08	5.94E-08	**6.94E-08**
FF1	2.23E-08	2.16E-08	2.10E-08	2.05E-08	2.02E-08	**2.36E-08**
FF2	2.71E-08 *	2.62E-08 *	2.54E-08 *	2.46E-08 *	2.39E-08 *	**2.37E-08**
TOUT1	5.15E-08	5.06E-08	4.97E-08	4.91E-08	4.86E-08	**5.45E-08**
TOUT5	4.79E-08	4.71E-08	4.65E-08	4.59E-08	4.54E-08	**1.07E-07**
DCE0	8.66E-08	8.38E-08	8.14E-08	7.92E-08	7.73E-08	**8.66E-08**
DCE1	6.59E-08	6.39E-08	6.25E-08	6.12E-08	6.01E-08	**8.73E-08**
DCE2	7.76E-08	7.60E-08	7.47E-08	7.36E-08	7.26E-08	**8.65E-08**
DCE3	7.89E-08	7.74E-08	7.61E-08	7.50E-08	7.40E-08	**8.67E-08**
DCE4	8.34E-08	8.05E-08	7.78E-08	7.57E-08	7.38E-08	**8.60E-08**
DCE5	6.40E-08	6.23E-08	6.09E-08	5.94E-08	5.82E-08	**8.67E-08**
DCE6	6.59E-08	6.35E-08	6.15E-08	5.96E-08	5.81E-08	**8.68E-08**
DCE7	6.54E-08	6.31E-08	6.10E-08	5.92E-08	5.77E-08	**8.64E-08**
DCE8	5.60E-08	5.44E-08	5.30E-08	5.19E-08	5.08E-08	**6.24E-08**
DCE9	5.61E-08	5.44E-08	5.31E-08	5.19E-08	5.08E-08	**6.07E-08**
DCE10	5.33E-08	5.18E-08	5.05E-08	4.93E-08	4.83E-08	**6.01E-08**
DCE11	5.74E-08	5.58E-08	5.44E-08	5.32E-08	5.21E-08	**6.13E-08**
DCE12	5.51E-08	5.35E-08	5.21E-08	5.10E-08	4.99E-08	**5.97E-08**
DCE13	5.72E-08	5.56E-08	5.42E-08	5.30E-08	5.20E-08	**6.10E-08**
DCE14	5.42E-08	5.26E-08	5.13E-08	5.01E-08	4.90E-08	**6.26E-08**
DCE15	6.05E-08	5.86E-08	5.72E-08	5.59E-08	5.48E-08	**6.36E-08**
DCE16	6.05E-08	5.83E-08	5.65E-08	5.49E-08	5.36E-08	**6.44E-08**
DCE17	6.29E-08	6.06E-08	5.87E-08	5.71E-08	5.57E-08	**6.57E-08**
DCE18	5.95E-08	5.72E-08	5.55E-08	5.39E-08	5.25E-08	**6.41E-08**
DCE19	6.02E-08	5.84E-08	5.72E-08	5.60E-08	5.49E-08	**6.29E-08**
DCE20	6.27E-08	6.06E-08	5.88E-08	5.75E-08	5.63E-08	**6.41E-08**
DCE21	6.18E-08	5.94E-08	5.78E-08	5.66E-08	5.56E-08	**6.45E-08**
DCE22	6.36E-08	6.16E-08	6.01E-08	5.86E-08	5.73E-08	**6.51E-08**
DCE23	6.31E-08	6.10E-08	5.90E-08	5.75E-08	5.61E-08	**6.74E-08**
DCE24	5.48E-08	5.29E-08	5.12E-08	4.96E-08	4.83E-08	**5.70E-08**
DCE25	5.30E-08	5.11E-08	4.93E-08	4.79E-08	4.66E-08	**5.57E-08**
DCE26	5.22E-08	5.10E-08	4.97E-08	4.87E-08	4.78E-08	**5.63E-08**
DCE27	5.52E-08	5.31E-08	5.16E-08	5.02E-08	4.89E-08	**5.60E-08**
DCE28	5.59E-08 *	5.42E-08	5.28E-08	5.16E-08	5.05E-08	**5.50E-08**
DCE29	5.61E-08 *	5.42E-08	5.25E-08	5.12E-08	4.98E-08	**5.58E-08**
DCE30	5.53E-08	5.35E-08	5.17E-08	5.03E-08	4.90E-08	**5.56E-08**
DCE31	5.85E-08	5.65E-08	5.48E-08	5.34E-08	5.21E-08	**6.16E-08**
DCE32	7.58E-08 *	7.32E-08	7.08E-08	6.87E-08	6.70E-08	**7.54E-08**
DCE33	6.36E-08	6.17E-08	6.02E-08	5.88E-08	5.76E-08	**6.86E-08**
DCE34	7.57E-08 *	7.31E-08 *	7.08E-08 *	6.88E-08	6.78E-08	**7.02E-08**

DCE35	6.53E-08	6.35E-08	6.18E-08	6.02E-08	5.88E-08	**6.91E-08**
DCE36	7.23E-08	6.97E-08	6.83E-08	6.70E-08	6.59E-08	**7.27E-08**
DCE37	6.12E-08	5.92E-08	5.78E-08	5.65E-08	5.53E-08	**6.30E-08**
DCE38	6.42E-08 *	6.17E-08	5.94E-08	5.75E-08	5.62E-08	**6.31E-08**
DCE39	6.26E-08	6.07E-08	5.89E-08	5.75E-08	5.62E-08	**6.60E-08**
MOUT40	7.74E-08	7.49E-08	7.28E-08	7.09E-08	6.92E-08	**8.40E-08**
MOUT41	8.57E-08	8.28E-08	8.02E-08	7.76E-08	7.56E-08	**9.10E-08**
MOUT42	8.83E-08	8.63E-08	8.47E-08	8.33E-08	8.20E-08	**9.67E-08**
MOUT43	8.91E-08	8.63E-08	8.39E-08	8.18E-08	8.01E-08	**1.00E-07**
MOUT44	9.01E-08	8.71E-08	8.48E-08	8.26E-08	8.09E-08	**9.85E-08**
MOUT45	8.73E-08	8.44E-08	8.17E-08	7.93E-08	7.74E-08	**9.22E-08**
MOUT46	7.77E-08	7.48E-08	7.26E-08	7.07E-08	6.89E-08	**8.92E-08**
MOUT47	7.81E-08	7.56E-08	7.33E-08	7.14E-08	6.98E-08	**9.00E-08**

Tin Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
TOUT1	2.80E-08	2.69E-08	2.61E-08	2.54E-08	2.48E-08	**3.15E-08**
TOUT5	6.71E-08	6.46E-08	6.25E-08	6.07E-08	5.90E-08	**8.76E-08**

Comb_test Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
SEL1	8.28E-08	8.01E-08	7.78E-08	7.60E-08	7.42E-08	**0.00000015**
SEL2	3.08E-08	2.95E-08	2.84E-08	2.75E-08	2.68E-08	**0.00000015**
SEL3	3.42E-08	3.27E-08	3.17E-08	3.06E-08	2.97E-08	**0.00000015**
SEL4	4.75E-08	4.58E-08	4.43E-08	4.30E-08	4.20E-08	**0.00000015**
RESET	1.17E-07	1.13E-07	1.10E-07	1.08E-07	1.06E-07	**0.00000015**

Set_up Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
Q0	1.49E-08	1.47E-08	1.44E-08	1.42E-08	1.40E-08	**-20/+50 E-9**
Q1	1.84E-08	1.82E-08	1.77E-08	1.75E-08	1.73E-08	**-20/+50 E-9**
Q2	1.31E-08	1.31E-08	1.29E-08	1.27E-08	1.25E-08	**-20/+50 E-9**
Q3	1.73E-08	1.69E-08	1.66E-08	1.64E-08	1.62E-08	**-20/+50 E-9**
LOAD	1.80E-08	1.72E-08	1.66E-08	1.60E-08	1.56E-08	**-20/+50 E-9**

Hold Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
Q0		-1.80E-08	-1.77E-08	-1.77E-08	-1.77E-08	**-40e-9/0**
Q1	-2.46E-08	-2.43E-08	-2.43E-08	-2.41E-08	-2.41E-08	**-40e-9/0**
Q2	-1.70E-08	-1.67E-08	-1.65E-08	-1.65E-08	-1.63E-08	**-40e-9/0**
Q3	-2.19E-08	-2.16E-08	-2.14E-08	-2.11E-08	-2.09E-08	**-40e-9/0**
LOAD	-1.41E-08	-1.33E-08	-1.28E-08	-1.23E-08	-1.19E-08	**-40e-9/0**

Pulse width Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
CLKIN	1.84E-08	1.83E-08	1.81E-08	1.80E-08	1.80E-08	**0.00000005**

Pulse width Params: Ins = 3.00V/0.00V

VCC	4.5	4.75	5	5.25	5.5	**LIMIT**
RESET	2.96E-08	2.91E-08	2.85E-08	2.81E-08	2.77E-08	**0.00000005**

DEVICE FAILED 4 TEST(S) @ 5V

SECTION 2.6
Life Test Results

JPL/HUGHES AIRCRAFT DATA SUMMARY

ACTEL 1020 FPGA 2000 hours LIFE TEST RESULTS

PARAMETRIC RESULTS

TEMP: -55°C TO 125°C

VCC: 4.50V TO 5.50V

	VOH	VOL	ISB	IIL	IIH	IOZL	IOZH	IOS	IOSP	VIH	VIL
Unit #1	control	control	control	control	control	control	control	control	control	control	control
Unit #2	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #3	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #4	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #5	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #6	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #7	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #7	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #8	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #9	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #10	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Unit #11	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass	pass
Max Limit	5.50V	400mv	25ma	10ua	10ua	10ua	10ua	-100ma	140ma	2.00v	2.00v
Max Value	5.2617v	129.6mv		0.305na	7.9na	0.85na	8.3na	-19.5ma	87.62ma	1.65v	1.4922v
Min Limit	3.7v	0.00v		-10ua	-10ua	-10ua	-10ua	-10ma	20ma	0.800v	0.800v
Min Value	4.154v	92.96mv	0ma	-0.7na	-0.2na	-1.0na	-1.0na	-33.5ma	55.3ma	1.2617v	1.041v
	ALL UNITS PASSED TEMPERATURE AND VOLTAGE RANGE										

SEM PHOTO VIEWS OF (ACT 1020B-SN10 FPGA WITH 2000 HRS LIFE TEST) CHIP CIRCUIT SEGMENT WITH EXPOSED METAL-2 AND METAL-1 CONTACTS WITH VOIDS, (TOP NITRIDE AND SiO_2 PASSIVATION REMOVED).

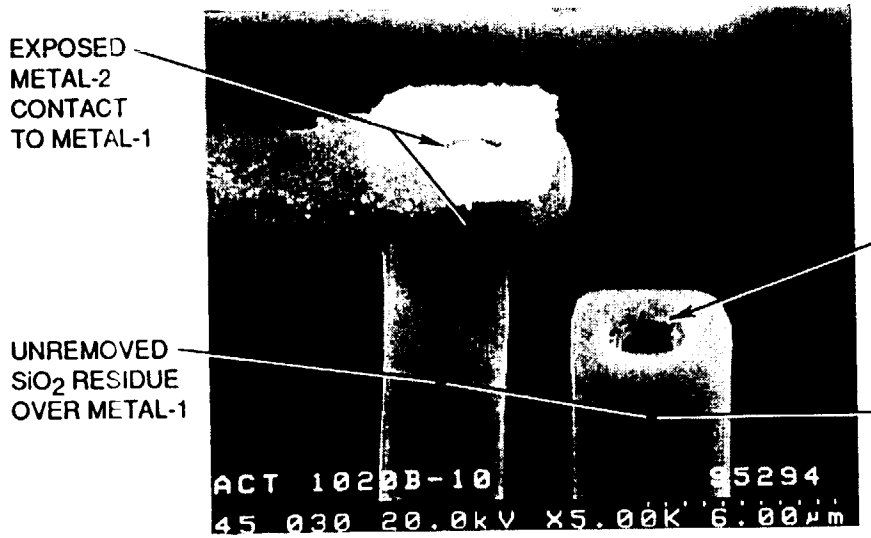

Figure 1a. 5kX view of exposed metal-1 contact to Si.

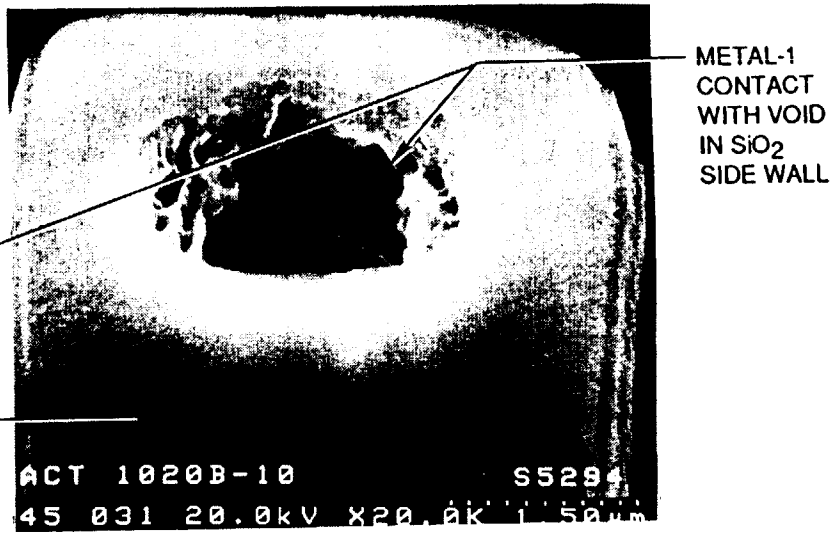

Figure 1b. 20kX magnified view of metal-contact to Si with void over SiO_2 via step cut.

Figure 2a. 8kX view of exposed metal-2 contacts to metal-1. (intrametal SiO_2 removed).

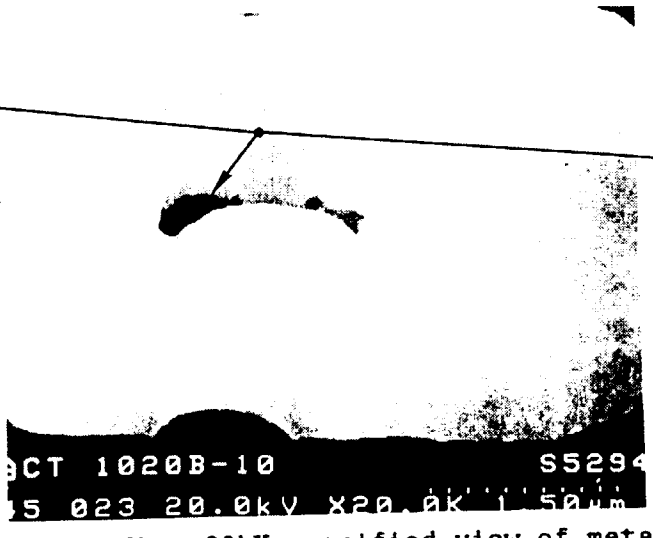

Figure 2b. 20kX magnified view of metal-2 contact to metal-1 with void over SiO_2 via step cut.

C-2

SECTION 2.7
Anomalous Behavior of Device Inputs

The Johns Hopkins University
Applied Physics Laboratory
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S2F-92-0101
March 30, 1992

TO: W. S. Devereux (HADR9BFXSOR)

FROM: R. C. Moore

SUBJECT: Anomalous Behavior of Actel 1020 FPGA Inputs

During checkout of the first EGTT engineering and GSE models we have discovered what appears to be a potential applications problem with logic inputs of the Actel A1020 2000-gate field-programmable gate array (FPGA). The problem involves inputs that behave briefly as outputs during power turn-on. This memorandum documents our findings to date, indicates certain applications that may be vulnerable to the effects of this problem, and indicates the steps I recommend to avoid those effects.

During power-on, the +5V logic supply rail of a flight electronics system typically rises from 0V to +5V in 50 ms or less. Because the regulator output is current-limited during this transition, the rise is more or less linear, with a slope in the range from 0.1 V/ms to 5 V/ms. The Actel 1020 FPGA has a universal pad driver design that may be configured as an input, output, three-state output, or bi-directional input/output. This configuration of the pad driver is accomplished by programming "anti-fuses" in the pad driver circuitry. Unfortunately, as the +5V logic supply rail passes through the region from approximately 2.2V through 2.5V, pad drivers that have been programmed as inputs may behave temporarily as outputs that are in the logic-H state. These input pins therefore will temporarily source current (approximately 8–10 mA, if not otherwise limited) into whatever driver is connected to them. They will be sourcing this current from the +5V logic rail, which at this time is at 2.2–2.5 volts.

The duration of this input anomaly is a function of the power rail rise time. For +5V rails that come up quickly, at 5 V/ms, the duration of the problem will be only ~60 µs. For supply rails that rise slowly, at 0.1 V/ms, the duration of the problem will be 3 ms. In the former case, the Actel 1020 input can deliver as much as 0.6 µC to the circuit that drives it; in the later case, the charge is as much as 30 µC. For many driver circuits, this amount of charge is insignificant; however, for others it can be quite upsetting.

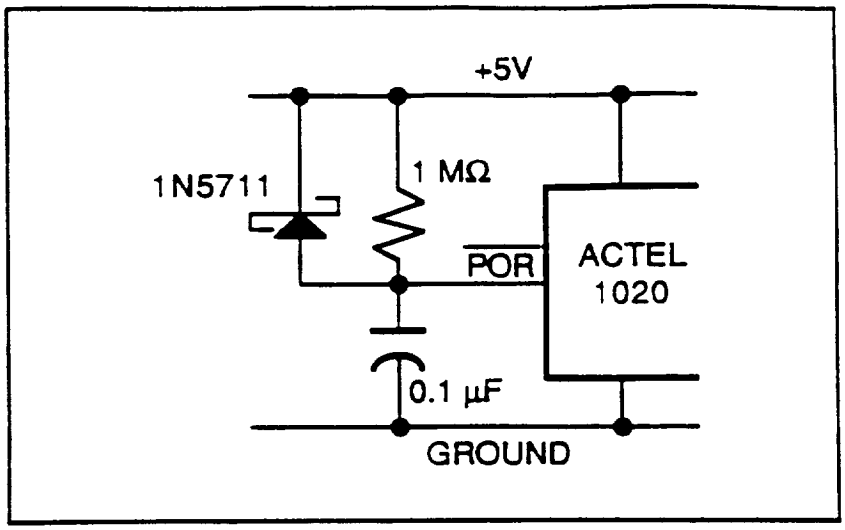


Figure 1: Typical POR Circuit for CMOS FPGA

Consider, for example, the typical power-on reset (POR) circuit of Figure 1. A capacitor is charged through a resistance to the +5V logic supply rail, using a time constant that is larger than the supply rail rise time, so that the input to the Actel 1020 is briefly at logic L during power-on, then remains at logic H until power-off. A diode across the resistor is used to discharge the POR capacitor at power-off. Using the 0.1 µF capacitance shown in Figure 1, 10 mA of unexpected current out of the Actel 1020 input will result in a voltage rise rate on the capacitor of $\Delta v/\Delta t = i/C = 0.1$ V/µs. If the logic supply rail takes at least 25 µs to pass through the range from 2.2V to 2.5V, the Actel input anomaly will charge the POR capacitor to almost 2.5V during power-on. This is enough to place _POR at a logic H for the rest of the power supply rail rise time, thereby defeating the intent of the circuit designer. Clearly, in this case at least, this is an unadvertised "feature" of the Actel 1020 input that is definitely not desirable!

This problem has an easy solution: insert a series resistance in the Actel input line of sufficient size to limit the effect of the anomaly to a safe value. In the case of the POR circuit, the series resistance must be chosen so as to keep $\Delta v \leq 1$V (to guarantee that _POR remains at a logic L following the anomaly, when the logic supply rail is at ~2.5V). For a power rail rise rate of 0.1 V/ms, for example, the anomaly duration will be about 3 ms. This means that, for a POR capacitance of 0.1 µF, the current out of the Actel 1020 input must be limited to $i = C\ \Delta v/\Delta t = 0.1$ µF · 1 V / 3 ms = 33 µA. This can be achieved using a resistance of 2.24 V/33 µA = 68 kΩ.

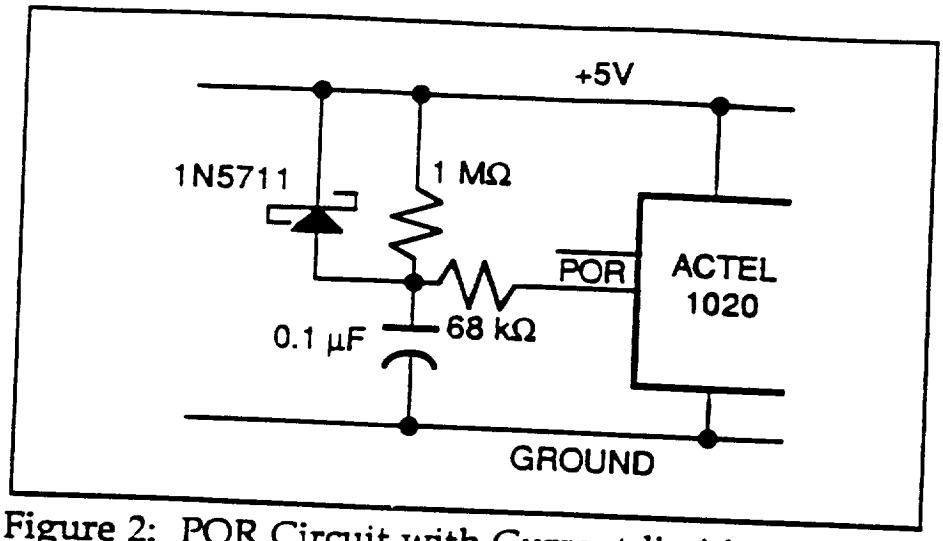


Figure 2: POR Circuit with Current-limiting Resistor

Figure 2 shows the additional circuitry. This circuit has been tested, and it does indeed eliminate the problem. By the way, if you try to duplicate this problem at your workbench, be advised that the Actel 1020 will not exhibit the anomaly unless its internal nodes have fully discharged. If the power rail has been turned off (0 volts on the +5V rail) for less than about ten minutes, at room temperature, the anomaly will not occur. (I first noticed this problem when our system was turned on after being off overnight.) As the supply rail rises from 2.2V to 2.5V you will also notice a significant rise in Actel 1020 supply current, typically as much as 50–60 mA above normal. This rise in supply current should pose no great problem for the typical +5V regulator, but be sure you de-couple the Actel 1020 locally.

If you are driving an Actel 1020 input with a driver that doesn't like to see a source of current at its output, or if you have Actel 1020 inputs that connect to a multiple-source data bus (a bus that may be driven by multiple three-state output drivers), I strongly recommend that the bus driver(s) be three-stated during POR. This could save you days of frustrating trouble-shooting.

Robert C. Moore

Robert C. Moore
EGTT Baseband Design

SECTION 2.8
Radiation Data Dose Rate
(See Subsection 3.1)

SECTION 3.0
Actel 1280 (1.2 µm)

SECTION 3.1
Radiation Data Dose Rate (ACT I&II)
(Magnavox)

MAGNAVOX ELECTRONIC SYSTEMS REPORT DOSE RATE TEST

PRODUCT: CMOS FIELD PROGRAMMABLE GATE ARRAY

MANUFACTURING BY: MATSUSHITA

DEVICE: A1020 2 MICRON & A1280 1.2 MICRON

EVALUATED BY: MAGNAVOX ELECTRONICS SYSTEMS COMPANY

REF: DOSE RATE TEST REPORT FOR THE ACTEL 1 & 11 ASIC's, MARCH 1992

1. ABSTRACT

Actel Corporation's ACT I (A1020) and ACT II (A1280) CMOS ASICs were dose rate tested at the Rockwell Autonetics Radiation Lab in Anaheim, CA on February 21, 1992. Five ACT I and two ACT II devices were checked for dose rate induced upset (U) latchup (LU) and burnout (BO). Each sample was programmed so that 95% of its gates were utilized in a series of combinational logic so that no matter where in the series an upset occurred it could be observed on an output.

The ACT I devices were of the same variety: Actel part number A1020, Magnavox part number 6BI3 and LDC 9132. The ACT II devices (A1280, LDC ES9143) were programmed slightly different from each other: Magnavox part number F6D2 was programmed with 6 outputs; 5DE7 with 3.

None of the parts exhibited latchup or burnout through $\approx 3 \times 10^9$ rad(Si)/s (17 ns FWHM). However, 3 forms of upset observed in these devices: U1) An output voltage transient of greater than or equal to 1 V (somewhat arbitrary threshold, many circuits can tolerate more); U2) A lost or shortened output pulse; and U3) the output railed either HIGH or LOW and required a manual RESET to resume normal operation.

The ACT I exhibited a highest no U1 threshold of 1.14×10^8 rad(Si)/s (0.50/90%), 8.71×10^7 (0.99/90%); a highest no U2 threshold of 1.82×10^8 rad(Si)/s (0.50/90%), 5.19×10^7 (0.99/90%); and a highest no U3 threshold of 2.53×10^8 rad(Si)/s (0.50/90%), 1.87×10^7 (0.99/90%).

The low sample size of ACT II devices precludes any meaningful statistical manipulations. The one sample of F6D2 demonstrated a highest no U1 of 8.34×10^7 rad(Si)/s and a highest no U2 of 2.65×10^8 rad(Si)/s. U3 was not observed in the F6D2. The one sample of 5DE7 showed a highest no U1 of 8.52×10^7 rad(Si)/s and a highest no U2 and U3 of 3.43×10^8 rad(Si)/s.

2. RADIATION FACILITIES AND DOSIMETRY

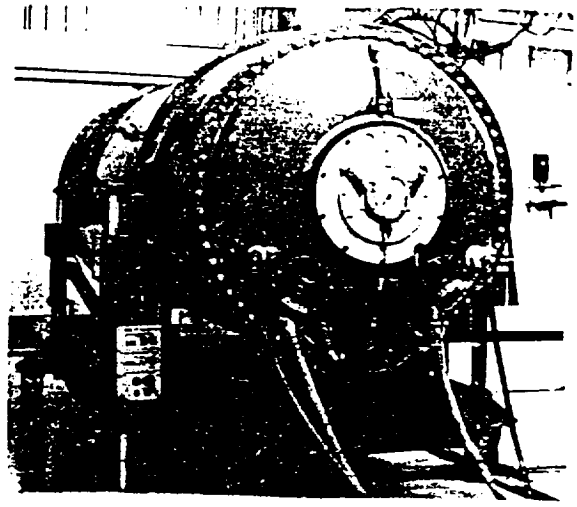
2.1 Source

Dose rate testing was performed at the Rockwell International Autonetics Division's Febetron 705 Flash X-Ray facility located in Anaheim, California. The Febetron 705 2.3 MeV FXR Machine, made by Hewlett Packard, was used to simulate transient ionization effects which produce photocurrents in semiconductors. The parts can be tested for upset threshold, latchup threshold, or survivability with varying radiation levels of the FXR pulse.

The FXR can be used to simulate electron beam energy or bremsstrahlung conversion into x-ray. The machine uses a bank of capacitors charged in parallel and discharged in series by means of spark gap switches. An electron beam is generated by discharging through a field-emission cathode vacuum tube. A magnetic coil around the discharge tube produces a magnetic field which focuses the electron beam. The anode material determines the mode of operation.

This test used the Febetron in the x-ray mode. In this mode, a tantalum plate is used to convert the electron beam energy into bremsstrahlung x-radiation. A maximum dose of 1 krad(Si) can be achieved. For the electron beam mode, the tantalum plate is removed and a beam collimator is attached. The maximum dose which can be obtained is 1 Mrad(Si). In both cases the radiation is delivered in a nominal 15 ns (FWHM). The Febetron 705 Flash X-Ray Machine and operating parameters are shown in Figure 2.1.1-1.

The dose rate can be adjusted by varying the distance between the object to be exposed and the FXR face plate. This is plotted in Figure 2.1.1-2 for both the electron beam and the x-ray modes. In the x-ray mode, the dose is a function of $1/d^2$ (d being the distance). Isodose contours are depicted in Figure 2.1.1-3. The exposure area also changes with distance; in the electron beam mode it ranges from 1/4" diameter at the face plate to a 12" diameter at 100 inches away (dose rate equal to 3×10^9 rad(Si)/s).



Flash X-Ray Parameters

Maximum Charging Voltage	35 kV
Maximum Electron Energy	2.3 MeV
Average Electron Energy	1.4 MeV
Total Beam Energy per Pulse	400 J
Maximum Pulse Repetition Rate	2 pulses/min
Pulse Width	15 ns (FWHM)

Electron Beam Mode

Maximum dose	1 Mrad(Si)
Dose Rate Range (1" to 100")	3×10^{13} to 1×10^{9} rad(Si)/s
Peak Electron Energy Fluence/Pulse	approx. 25 cal/cm^2

Flash X-Ray (Bremsstrahlung) Mode (Tantalum Target)

Maximum dose	1 krad(Si) (touching face plate, narrow beam)
Dose Rate (1" from face plate)	3×10^{9} rad(Si)/s
Mean Photon Energy	approx. 700 keV

Figure 2.1.1-1 Febetron 705 Flash X-Ray Machine

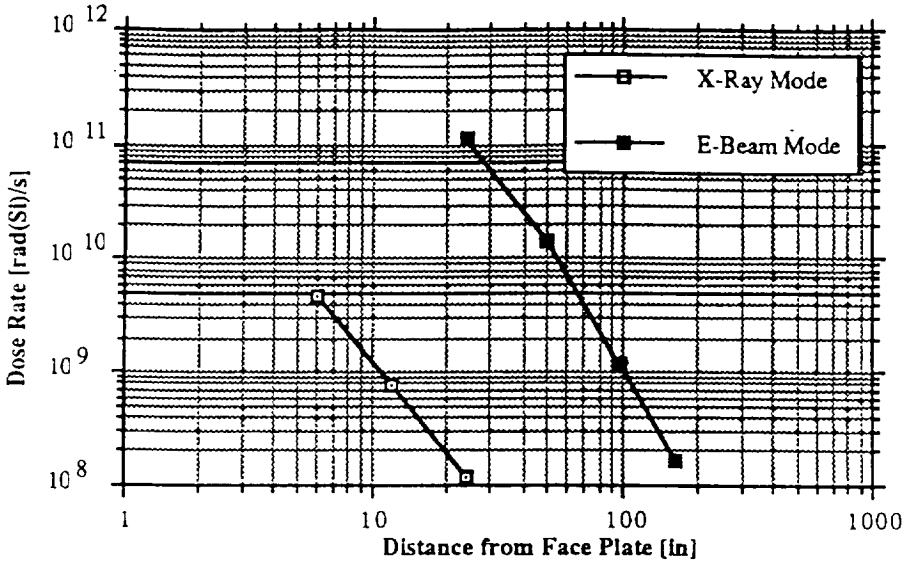
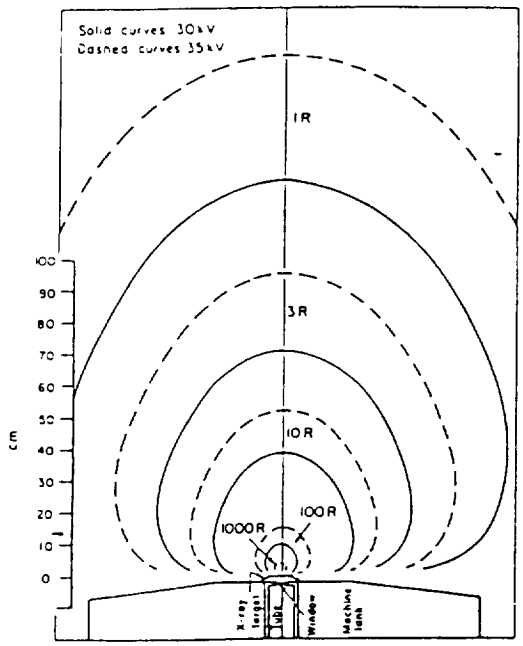


Figure 2.1.1-2 Flash X-Ray Dose Rate Variation with Distance



tube 54SC, 30- and 35-kV incident beams.

Figure 2.1.1-3 X-Ray Isodose Contour Map

The device under test (DUT) and support circuitry (loads, line drivers, etc.) are housed in an RF shielded enclosure. Support circuitry is further shielded by lead and aluminum laminations to minimize false signals. In support of FXR radiation testing, real time monitoring of the DUT is accomplished using the Digital Signal Analysis System which consists of nineteen transient waveform digitizers. These include Tektronix 7912AD and RTD710, and LeCroy 8828C and 6880A.

2.1.2 Dosimetry

Active dosimetry for measuring dose rate is provided at the Flash X-Ray source. Calibrated radiation detector diodes provide pulse waveforms that appear on a digitizer screen. Other dosimetry such as TLD and Calcium Fluoride capsule is also available as an option. The calibration of all sources are directly traceable to the National Institute of Standards and Technology.

4. TEST RESULTS

The ACT I (B6I3) and ACT II (F6D2 and 5DE7) test results are summarized in Tables 4.1-1, 4.1-2 and 4.1-3. Raw test data is presented in Appendix A-1 (B6I3), A-2 (F6D2) and A-3 (5DE7) in order of increasing sample number and increasing radiation level.

Table 4.1-1. ACT I Dose Rate Test Results.

Sample #	Dose Rate @ 15ns FWHM [rad(Si)/s]	Shot #	Upset Type: Transient 1	Transient [V]	Lost/Shortened 2	Rail 3	Rail Manual Reset	Latchup	Burnout	Comment
ACT I, B6I3 Actel A1020 CMOS ASIC (LDC = 9132, Sample Size = 5)										
1	6.26E+07	50	no	0.4	no	no	no	no	no	
	8.63E+07	51	no	0.7	no	no	no	no	no	
	1.28E+08	52	no	0.8	no	no	no	no	no	
	1.30E+08	1	no	0.8	no	no	no	no	no	
	3.90E+08	2	-	-	-	YES	YES	no	no	
2	5.89E+07	49	no	0.60	no	no	no	no	no	
	8.14E+07	48	no	0.70	no	no	no	no	no	
	1.25E+08	47	no	0.80	no	no	no	no	no	
	1.99E+08	13	YES	1.60	no	no	no	no	no	
	2.81E+08	14	YES	2.00	no	no	no	no	no	
	3.27E+08	16	-	-	YES	no	no	no	no	pulse shortened
	4.06E+08	15	-	-	-	YES	YES	no	no	
	2.80E+09	18	-	-	-	YES	YES	no	no	
	2.85E+09	17	-	-	-	YES	YES	no	no	
3	5.79E+07	44	no	0.40	no	no	no	no	no	
	8.90E+07	45	no	0.60	no	no	no	no	no	
	1.23E+08	46	no	0.80	no	no	no	no	no	
	2.41E+08	26	YES	1.60	no	no	no	no	no	
	2.74E+08	25	-	-	YES	no	no	no	no	pulse shortened
	3.79E+08	20	-	-	YES	no	no	no	no	pulse lost
	4.55E+08	21	-	-	YES	no	no	no	no	pulse shortened
	5.73E+08	22	-	-	YES	no	no	no	no	pulse lost
	9.29E+08	23	Not Likely	-	Maybe	no	no	no	no	upset masked†
	1.01E+09	24	-	-	-	YES	YES	no	no	
	2.78E+09	19	-	-	-	YES	YES	no	no	
4	=0	28	no	-	no	no	no	no	no	noise shot
	=0	29	no	-	no	no	no	no	no	noise shot
	9.73E+07	32	no	0.00	no	no	no	no	no	
	1.23E+08	31	no	0.90	no	no	no	no	no	
	1.99E+08	30	YES	1.60	no	no	no	no	no	
	2.44E+08	27	YES	1.80	no	no	no	no	no	
	2.78E+08	34	-	-	YES	no	no	no	no	pulse shortened
	3.82E+08	33	-	-	-	YES	YES	no	no	
	2.50E+09	35	Not Likely	-	Maybe	Not Likely	no	no	no	upset masked†
5	5.61E+07	43	no	0.30	no	no	no	no	no	
	8.26E+07	42	no	0.70	no	no	no	no	no	
	1.10E+08	41	no	0.80	no	no	no	no	no	
	1.23E+08	40	YES	1.40	no	no	no	no	no	
	2.71E+08	39	YES	1.90	no	no	no	no	no	
	3.07E+08	38	-	-	YES	no	no	no	no	pulse shortened
	3.65E+08	37	-	-	-	YES	YES	no	no	
	2.80E+09	36	-	-	-	YES	YES	no	no	

† Dose rate occurred on H to L transision and may have masked the upset.
Upset 1 (U1) is a output voltage transient of greater than or equal to 1 V.
Upset 2 (U2) is a lost or shortened output pulse
Upset 3 (U3) is where the output railed either HIGH or LOW and a manual RESET was required to resume operation.

Table 4.1-2. ACT II Dose Rate Test Results.

Sample #	Dose Rate @ 15ns FWHM [rad(Si)/s]	Shot #	Upset Type: Transient 1	Transient [V]	Lost/Shortened 2	Rail 3	Rail Manual Reset	Latchup	Burnout	Comment
ACT II, F6D2 6 output Actel A1280 CMOS ASIC (LDC = ES9143, Sample Size = 1)										
1	5.80E+07	55	no	0.60	no	no	no	no	no	
	8.34E+07	54	no	0.80	no	no	no	no	no	
	1.26E+08	3	YES	1.20	no	no	no	no	no	
	1.26E+08	53	YES	1.10	no	no	no	no	no	
	2.06E+08	5	YES	1.80	no	no	no	no	no	
	2.60E+08	57	YES	2.00	no	no	no	no	no	
	2.67E+08	58	YES	2.20	no	no	no	no	no	
	3.90E+08	4	-	-	YES	no	no	no	no	pulse shortened
	2.60E+09	6	-	-	YES	no	no	no	no	pulse lost
ACT II, 5DE7 3 output Actel A1280 CMOS ASIC (LDC = ES9143, Sample Size = 1)										
1	6.09E+07	61	no	0.80	no	no	no	no	no	
	8.52E+07	60	no	0.80	no	no	no	no	no	
	1.25E+08	59	YES	1.00	no	no	no	no	no	
	2.09E+08	9	YES	1.80	no	no	no	no	no	
	2.84E+08	10	YES	2.40	no	no	no	no	no	
	3.43E+08	11	YES	2.80	no	no	no	no	no	
	3.91E+08	8	-	-	-	YES	YES	no	no	
	4.00E+08	12	-	-	-	YES	YES	no	no	
	2.71E+09	7	-	-	YES	no	no	no	no	pulse shortened

Upset 1 (U1) is a output voltage transient of greater than or equal to 1 V.
Upset 2 (U2) is a lost or shortened output pulse
Upset 3 (U3) is where the output railed either HIGH or LOW and a manual RESET was required to resume operation.

Table 4.1-3. ACT I and ACT II Dose Rate Test Results Summary.

Device Type	Part #	Sample #	Highest No U1	Lowest U1	Highest No U2	Lowest U2	Highest No U3	Lowest U3
Data summary for all ACT I and ACT II devices								
ACT I	B6I3	1	-	-	1.30E+08	3.90E+08	-	-
		2	1.25E+08	1.99E+08	2.81E+08	3.27E+08	3.27E+08	4.06E+08
		3	1.23E+08	2.41E+08	2.41E+08	2.74E+08	9.29E+08	1.01E+09
		4	1.23E+08	1.99E+08	2.44E+08	2.78E+08	2.78E+08	3.82E+08
		5	1.10E+08	1.23E+08	2.71E+08	3.07E+08	3.07E+08	3.65E+08
ACT II	F6D2	1	8.34E+07	1.26E+08	2.65E+08	3.90E+08	-	-
	5DE7	1	8.52E+07	1.25E+08	3.43E+08	2.71E+09	3.43E+08	3.91E+08

			LN(No U1)	LN(No U2)	LN(No U3)
Log normal statistical manipulation of ACT I results					
ACT 1	B6I3	1	-	1.87E+01	-
		2	1.86E+01	1.95E+01	1.96E+01
		3	1.86E+01	1.93E+01	2.06E+01
		4	1.86E+01	1.93E+01	1.94E+01
		5	1.85E+01	1.94E+01	1.95E+01
		Mean	1.86E+01	1.92E+01	1.98E+01
		Std Dev	5.90E-02	3.15E-01	5.64E-01
k(4)=0.819; k(5)=0.686		0.50/90%	1.86E+01	1.90E+01	1.93E+01
k(4)=5.437; k(5)=4.666		0.99/90%	1.83E+01	1.78E+01	1.67E+01
		exp(0.50/90%)	**1.14E+08**	**1.82E+08**	**2.53E+08**
		exp(0.99/90%)	**8.71E+07**	**5.19E+07**	**1.87E+07**

SECTION 3.1
Radiation Data Dose Rate (ACT I&II)
(TRW)

1.0 INTRODUCTION

This document reports results for gamma-rate response testing of a specific configuration of ACTEL 1280 Gate Arrays in a Flash X-ray (FXR) environment.

The parts were tested using the TRW Febetron FXR machine. The FWHM pulse width was 22 nanoseconds.

The primary objective was to test for burnout at the highest available levels while noting if any latchup had occurred. A secondary objective was to collect upset data.

2.0 TEST SAMPLES

The test samples were identified as ACTEL A1280 PG176 E3, lot date code 9143. Four samples were irradiated. These were identified as SN 1, SN 2, SN 3 and SN 4.

The arrays were configured with two different paths for data flow as shown in Figure 1. These paths were essentially constructed as rings of 32-bit shift register blocks sharing a reset circuit (note reset flip-flop). While separate clock lines were available, the input pins were wired together for these tests. Path 1 whose outputs have been labeled A and B had seventeen shift register blocks. Path 2 (outputs A′ and B′) had eight register blocks. Note that the 32-bit register block in the two paths were built differently. Additional details can be obtained from the TRW Components Engineering Department.

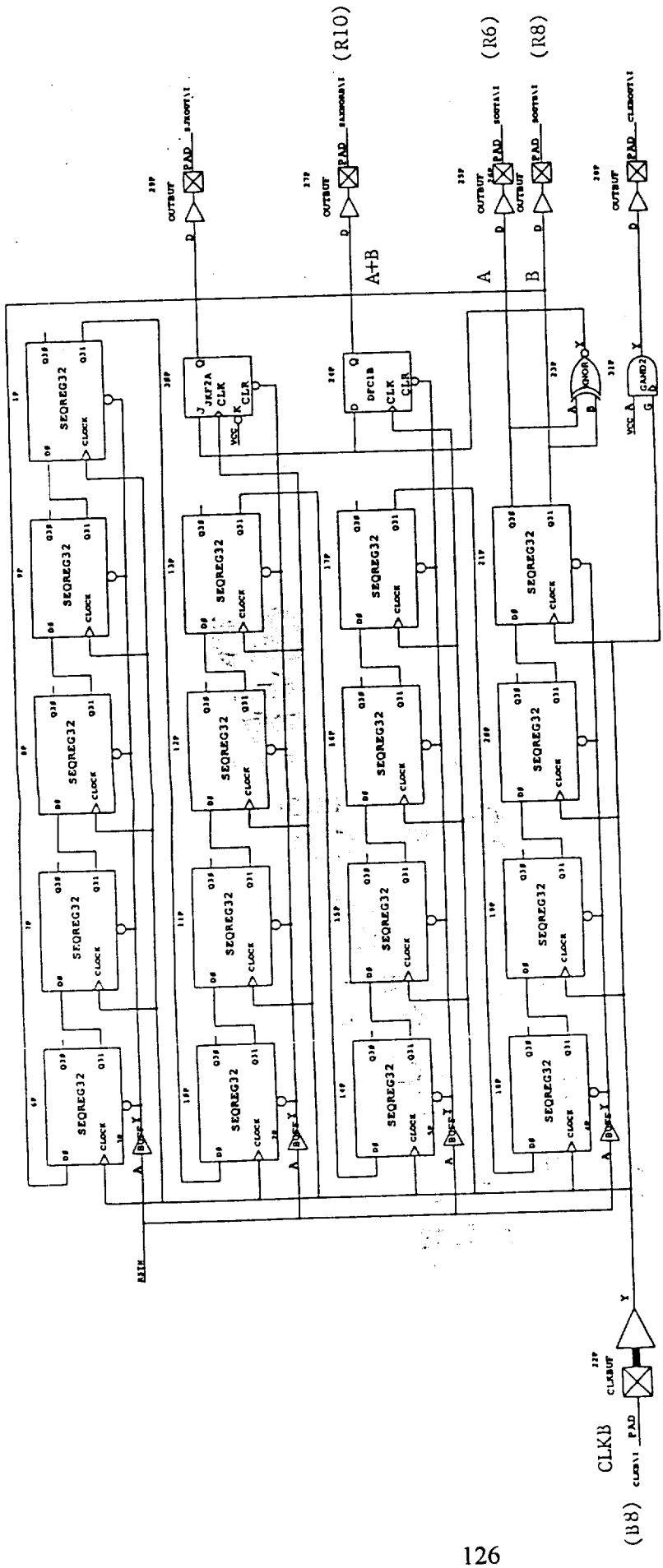
3.0 TEST DESCRIPTION

The test system configuration is shown in Figure 2.

All tests were conducted at laboratory ambient temperature with VCC = 5.0V. Both static and dynamic exposures were obtained. When a clock was used, the period was approximately 7 milliseconds with a clock pulse level of 4 volts and a width of 2 milliseconds.

The VCC line was stiffened with 200 ufd of capacitance located approximately eight inches from the DUT card and shielded with lead. Additionally, two 4.7 ufd ceramic capacitors were connected between the VCC pin and the DUT card ground plane.

A CT-2 AC current probe was used to obtain transient current photographs. When the DUT peak photo currents were recorded, the CT-2 was moved from its normal location (as shown in Figure 2) to the DUT side of the 4.7 ufd capacitors. However, for the actual burnout and latchup tests, the CT-2 was on the supply side of the 4.7 ufd capacitors in order to provide maximum stiffening.



PATH 1

FIGURE 1 - GATE ARRAY CONFIGURATION (SHEET 1 OF 2)

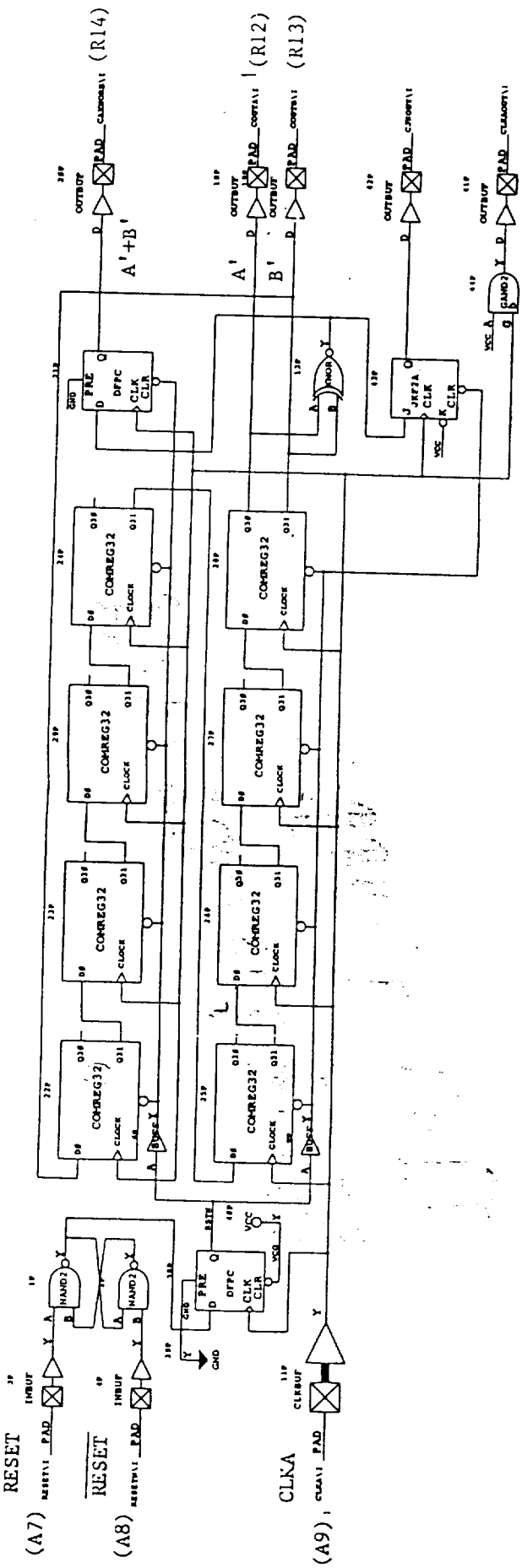
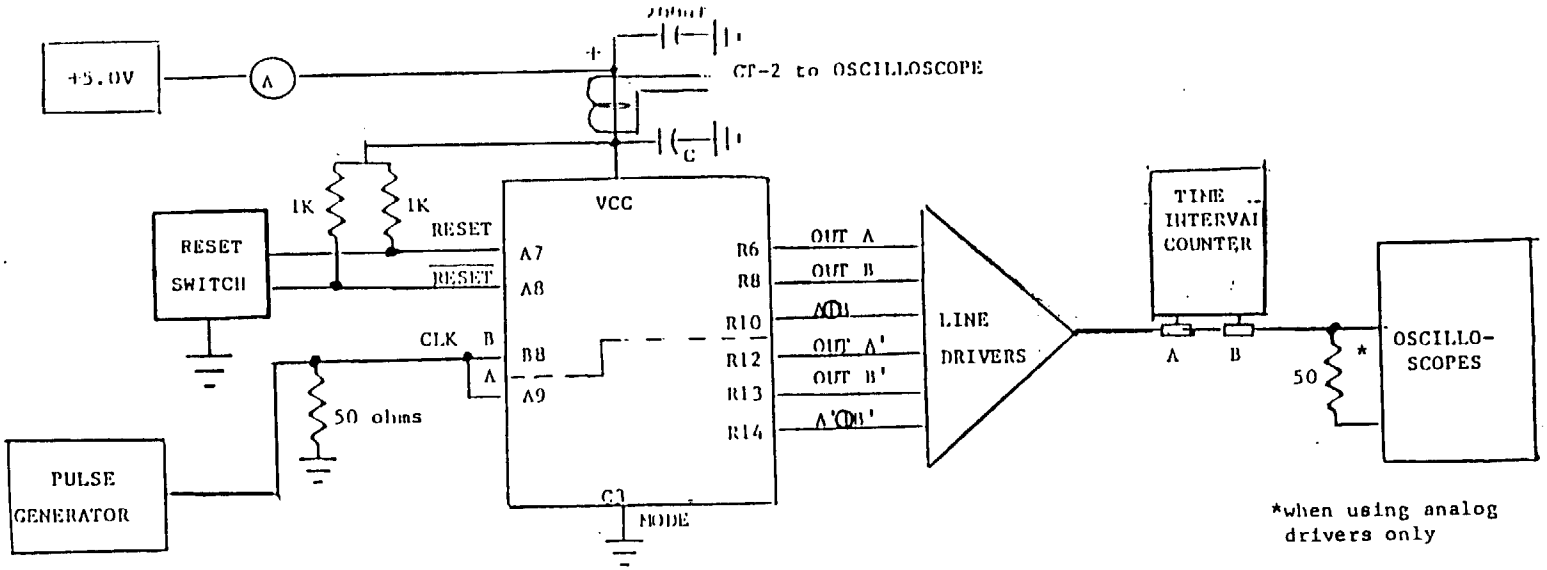


FIGURE 1 - GATE ARRAY CONFIGURATION (SHEET 2 OF 2)



NOTES:

1. DUT designators are pin grid locations. (See Appendix A).
2. VPP, VSV = VCC. VKS = GND. PRA, PRB, SDI, SDO, DCLK = N/C.
3. GND and VCC pins are per Appendix A.
4. C = Two 4.7ufd high frequency capacitors in parallel.
5. CT-2 located as shown except for selected shots where actual device transient current was to be measured.
6. Line drivers were either digital types located at the DUT and in the instrumentation room, or analog types located at the DUT. The analog drivers were used when investigating transient response levels (as opposed to data errors).
7. DUT circuit board and line drivers were located within RF cassette for upset tests.
8. Time interval counters were used to assist in detecting data errors.

FIGURE 2 - TEST SYSTEM BLOCK DIAGRAM

Line drivers located approximately twelve inches from the DUT and shielded with lead were used to monitor the output responses.

The tests were connected both with and without an RF type cassette enclosing the DUT card and line drivers.

4.0 TEST RESULTS

4.1 Upset Testing

Three types of "upset" were noted. These were:

a) transient output disturbance only

b) shortened output pulse (logic level transition coincided with the radiation pulse but with no additional data errors)

c) data errors evident after the pulse and reset therefore required

4.1.1 Transients and Shortened Pulses

The lowest gamma dose level capable of causing an output disturbance of approximately 1.3 volts but without the outputs transitioning was approximately 11 rads (5E8 rads/second).

With very little additional dose the outputs would transition coincident with the radiation, resulting in a single shortened pulse followed by the normal data stream. Figure 3 provides photographs for SN 1, Path 1 at 12 rads (5.5E8 rads/second).

4.1.2 Permanent Data Errors

All four parts were tested for this upset mode on Path 1. Only SN 3 and SN 4 were tested for this mode on Path 2.

Note that this upset mode may be expected to disappear at higher test levels since the on-chip reset flip-flop could generate its own reset. Thus, an apparent upset "window" could occur. This indeed was observed as the levels were increased and the need for a reset disappeared.

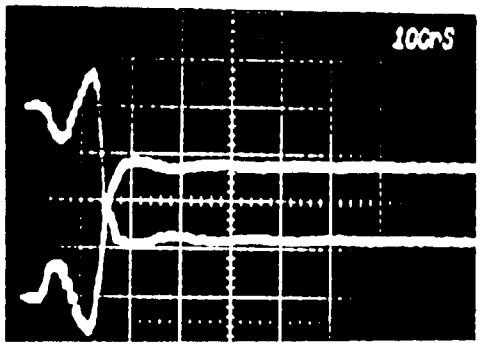
Table 1 provides key test levels that did or did not result in the need for a reset. There is some overlap in the levels and this could be related to a combination of dosimetry accuracy, DUT state sensitivity (e.g. clock high or clock low), and the presence of the on-chip reset circuitry. Nevertheless, the data are taken to indicate a threshold of 20-25 rads or approximately 1E9 rads/second.

Table 2 provides the data for Path 2. The threshold is apparently the same.

Figure 4 provides oscilloscope traces taken during and immediately after a 25 rad shot of SN 3. In this case, both paths had multiple data errors that lasted until a reset was applied.

Figure 5 provides oscilloscope traces taken during and immediately after a 30 rad shot of SN 3. In this case, Path 2 showed no lasting errors, but Path 1 was completely "shut down" or was circulating all zeroes. This result was observed several times. In all cases, the condition was cleared when the reset was applied.

1.8V, 100 nsecond/division



A High

B High

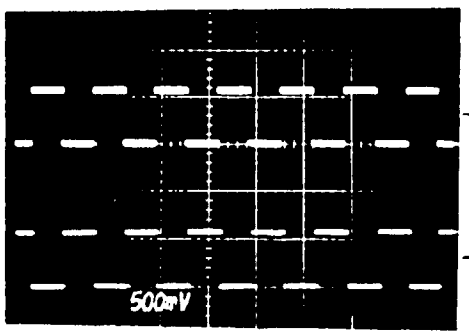
A Low

B Low

Radiation Pulse

Transition occurs at radiation pulse

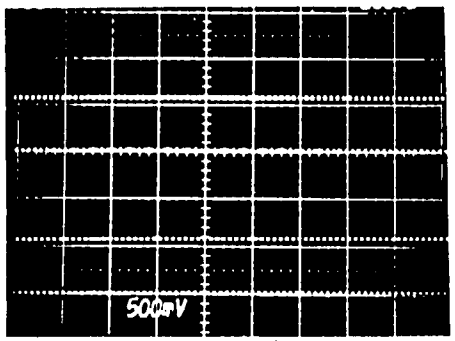
4.5V, 10 msecond/division



A

B

4.5V, 100 msecond/division



No Reset Required

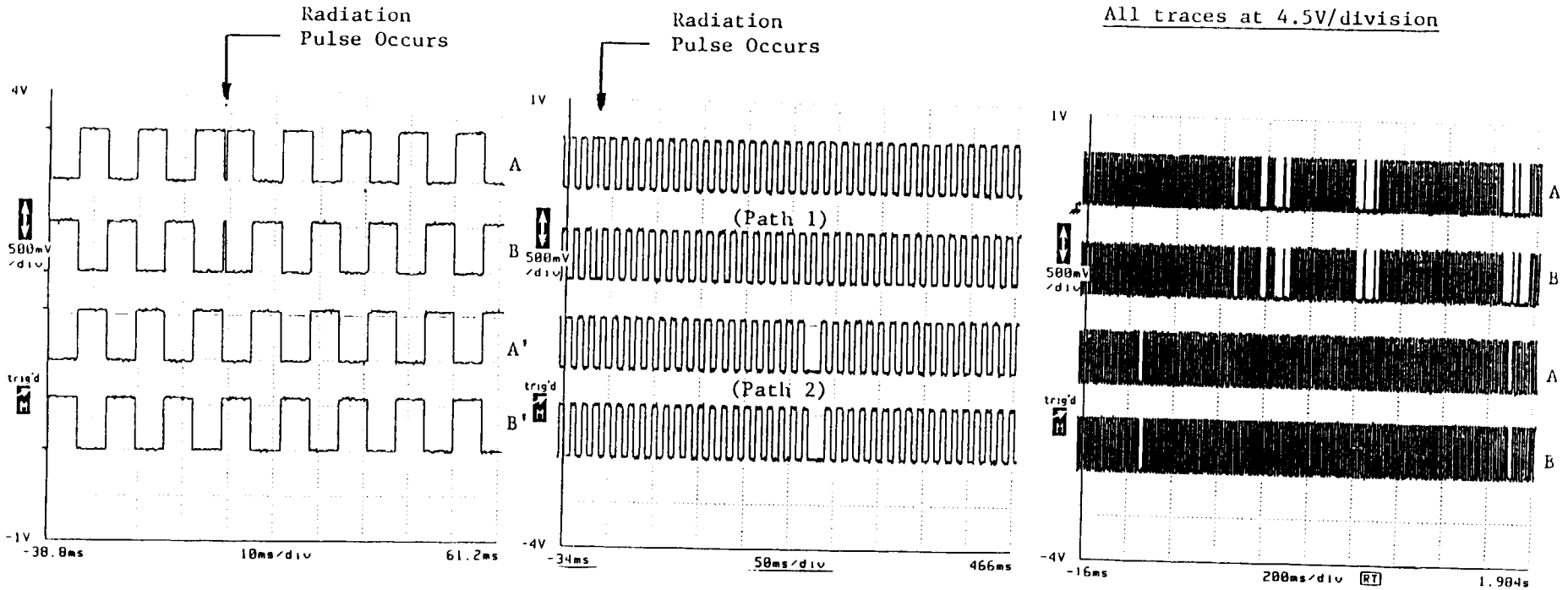
FIGURE 3 - SN 1, PATH 1 RESPONSE AT 12 RADS

TABLE 1 - UPSET DATA, PATH 1 PERMANENT DATA ERRORS

SN	No Reset Needed at (Rads)	Reset Needed at (Rads)	Notes
1	12, 17, 20, 22, 28	21, 32, 43, 45	
2	18, 25, 26	34, 35	
3	15, 18, 19, 25, 31, 32	25, 30, 33, 34, 41, 43	
4	15, 16, 21, 22, 23, 24, 25, 30, 35, 39, 40	32, 34, 36	

TABLE 2 - UPSET DATA, PATH 2 PERMANENT DATA ERRORS

SN	No Reset Needed at (Rads)	Reset Needed at (Rads)	Notes
3	15, 19, 25, 30, 31, 33, 37, 38	25, 44	
4	15, 16, 21, 25, 30, 34, 36, 40, 42	22, 23, 25	



Note A and A' are out of phase after shot.

Data error long after radiation pulse.

Data errors on Path 1 and Path 2 require reset.

FIGURE 4 - SN 3, PATH 1 AND PATH 2 RESPONSE AT 25 RADS

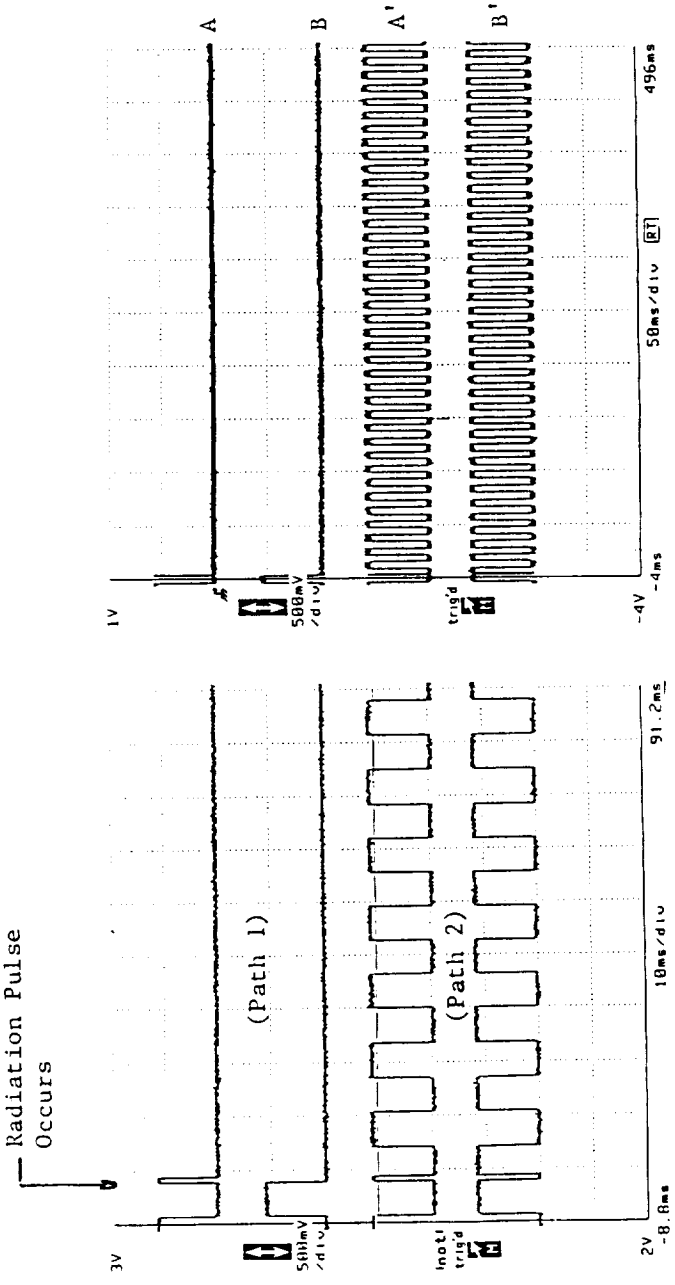


FIGURE 5 - SN 3, PATH 1 AND PATH 2 RESPONSE AT 30 RADS

4.2 Latchup/Burnout Testing

All four parts were exposed to a sequence of high level irradiations to check for latchup or burnout.

The supply voltage was 5.0V and no current limiting resistors were used.

All parts were tested to levels above 1E11 rads/second. Based upon the transient supply current waveforms, the pre- and post-exposure recordings of steady state current, and the photographs of the output waveforms, no latchup was observed. No obvious burnout damage occurred in that the parts were still functioning.

It should be noted that the high level pulses were observed to increase the values of the supply current for all four samples. The pre- and post-exposure values for ICC are given in Tables 3 and 4, along with the exposure levels. After each radiation pulse for which an increase in supply current was induced, it was noted that the level was slowly but continuously decreasing. In fact, approximately three weeks after SN 1 and SN 2 were exposed, their supply currents had decreased from 17mA and 59mA to 4.5mA and 20mA. Over the period of a weekend, SN 3 and SN 4 currents decreased from 7mA and 3mA to 3.6mA and 2.6mA. It may be that the observed increases are due to dose accumulation as opposed to photocurrent induced stressing.

Figure 6 provides supply current response photographs for SN 3 at 300, 1600 and 1950 rads or 1.4E10, 7.3E10 and 8.9E10 rads/second. The peak current was 9A at 300 rads and 15A at 1950 rads. The corresponding pulse widths were 150 nanoseconds and 350 nanoseconds.

TABLE 3 - LATCHUP/BURNOUT TEST LEVELS FOR SN 1 AND SN 2

SN	Test	Test Level Rads(Si)	ICC (mA)		Notes (1)
			Pre	Post	
1	1	803	0.9	1.1	
1	2	2355	1.0	1.0	
1	3	3355	2.1	5.4	
1	4	1866	3.1	7.0	
1	5	2026	9.4	8.0	
1	6	2900	8	17	(2)
2	7	533	0.0	0.0	
2	8	2400	0.0	3.0	
2	9	3236	0.1	6.0	
2	10	2170	3.0	16	(3)
2	11	920	14	26	(4)
2	12	1673	29	59	

NOTES:

1. For tests 1-5, 7-9 and 12 the dose readings are the average of two dosimeters located at the center of the DUT package lid.

2. For test 6, the value is the average of five dosimeters located at the corners and center of the package lid. The readings ranged from 2000-4000 rads.

3. The dose value is the average of two readings from opposite corners of the package lid. Readings were 2947 and 1396.

4. The dose value is the average of two readings from opposite corners of the package lid. Readings were 1130 and 707.

TABLE 4 - LATCHUP/BURNOUT TEST LEVELS FOR SN 3 AND SN 4

SN	Test	Test Level Rads(Si)	ICC (mA)		Remarks
			Pre	Post	
3	13	575	0.3	0.4	
3	14	1026	0.3	0.4	
3	15	314	0.4	0.4	
3	16	602	0.4	0.6	
3	17	1617	0.5	1.0	
3	18	1963	0.7	1.7	2413/1513
3	19	2795	1.7	3.2	2700/2890
3	20	1197	3.1	3.9	1269/1125
4	21	742	0.3	0.3	
4	22	750	0.3	0.4	
4	23	750	0.4	0.5	
4	24	750	0.6	0.7	
4	25	750	0.7	1.2	
4	26	750	1.2	1.7	
4	27	1382	1.0	1.7	
3	28	2922	3.6	7.0	2865/2980
4	29	2818	1.2	3.0	2875/2762
4	30	1075	2.6	3.6	
4	31	1836	3.1	4.0	1684/1988

Notes:

1. For shots 18-20, 28, 29 and 31, the level is the average for two dosimeter readings near the center of the device package lid. Individual readings are given under Remarks.

2. Shots 22-26 were made in rapid succession without moving the setup and a total dose of 3750 rads was obtained from a single reading.

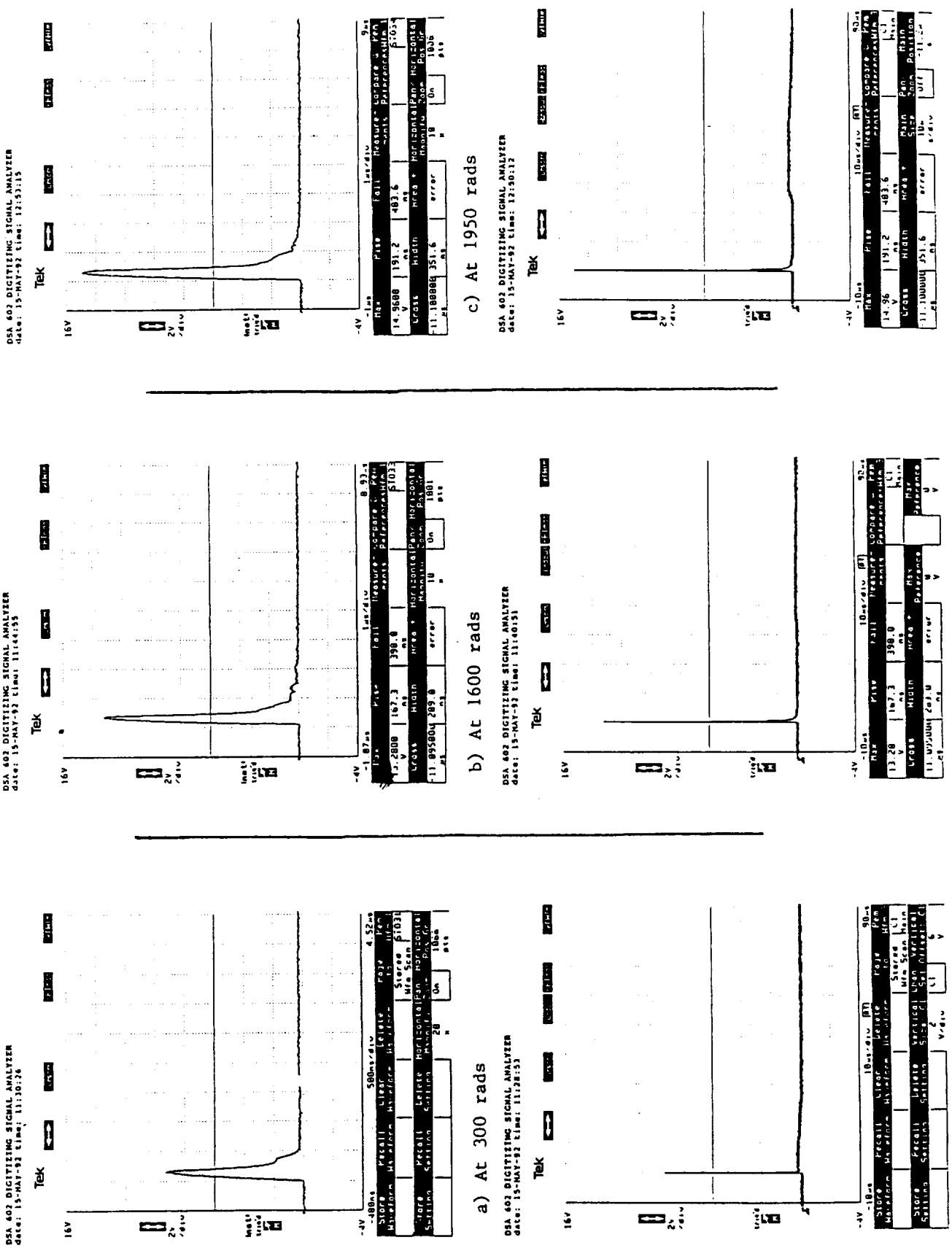


FIGURE 6 – ICC RESPONSE WAVEFORMS FOR SN 3

5.0 SUMMARY

This configuration of ACTEL 1280 gate arrays will upset at 5E8 rads/second (22 nanosecond pulse). At this level, either the output transients are sufficient to generate errors in downstream circuits, or the array outputs themselves may change state at the radiation pulse (but with no internal errors). At approximately 1E9 rads/second, internal errors are generated and a reset is necessary.

The four samples did not suffer any hard latchup and continued to function after levels above 1E11 rads/second where peak currents of 15A were generated. A small current limiting resistor should be used to reduce this photocurrent level.

The test samples should undergo a complete set of electrical measurements to ensure that parameters other than the operating current were not significantly degraded.

SECTION 3.2
Radiation Data SEU

AEROSPACE CORPORATION SUMMARY REPORT

PRODUCT: CMOS FIELD PROGRAMMABLE GATE ARRAY
MANUFACTURING BY: MATSUSHITA
DEVICE: ACT1010/ACT1020 (2.0 micron); ACT1280 (1.2 micron)
EVALUATED BY: AEROSPACE CORPORATION
Ref. (1)Single Event Effects Testing Report by R.Koga
Ref. (2)Single Event Upset and Latchup Susceptibilities of Actel A1280 CMOS Field Programmable Gate Array Report by R.Koga & S.J.Hansel

EVALUATIONS:

A1280 SINGLE EVENT UPSET (SEU) and LATCHUP SUSCEPTIBILITY

Data was taken on four devices each of which was programmed using four sequential ring counters and four combinatorial ring counters. Each device module was programmed as a multiple twisted ring counter using 60 D-type flip-flops. All programming was accomplished with antifuse elements. The programming was performed by ACTEL.

The test measurement was accomplished by by comparing the correct output signature of an unexposed device to the device that is exposed to the ion beam. Each device tested is exposed to a number of cycles while a sufficient number of output errors is accumulated and recorded. During exposure the power supply current was also monitored to detect latchup. SEU and latchup measurements were taken at room temperature and at 100°C.

Test results show that null latchup results were measured at the effective LET's ranging from 15 to 120 Mev/(mg/cm2). The SEU measurements were taken and plotted as (cm2/240 flip-flops) vs LET[MeV/(mg/cm2)]; See figure 3. Examination of the data shows that C-modules are less vulnerable than S-modues for SEU. At 100°C the results are identical.

A1010/A1020 SINGLE EVENT UPSET (SEU) and LATCHUP SUSCEPTIBILITY

The parts evaluated for SEU were exposed to Xe(603 MeV), Kr(380 MeV),Cu(290 MeV), and Ar (180 MeV) ion beams. They were programmed as multiple twisted ring counters each of which was 10 bits long. The A1010 and A1020 were programmed to hold four and five ring counters which contained 40 and 50 vulnerable bits.

The test measurement was done similarly as described for the A1280.

Test results show that null latchup results were measured at the effective LET's ranging from 15 to 120 Mev/(mg/cm2). The SEU measurements were taken and plotted as (cm2/ 40 or 50 flip-flops) vs LET[MeV/(mg/cm2)]. From the data it is seen that the A1010 and A1020 have similar susceptibilities. The test results at 80°C and 100°C are nearly identical to those at room temperature. Null latchup were measured at effective LETs ranging from 15 to 120 MeV/(mg/cm2). See figure 4 and 5.

Post SEU testing of antifuses at 100°C revealed some errors. However it is speculated these errors were the result of using commercial devices rated and tested to 70°C. There was also some indication of mishandling the parts after SEU testing.

Actel A1280

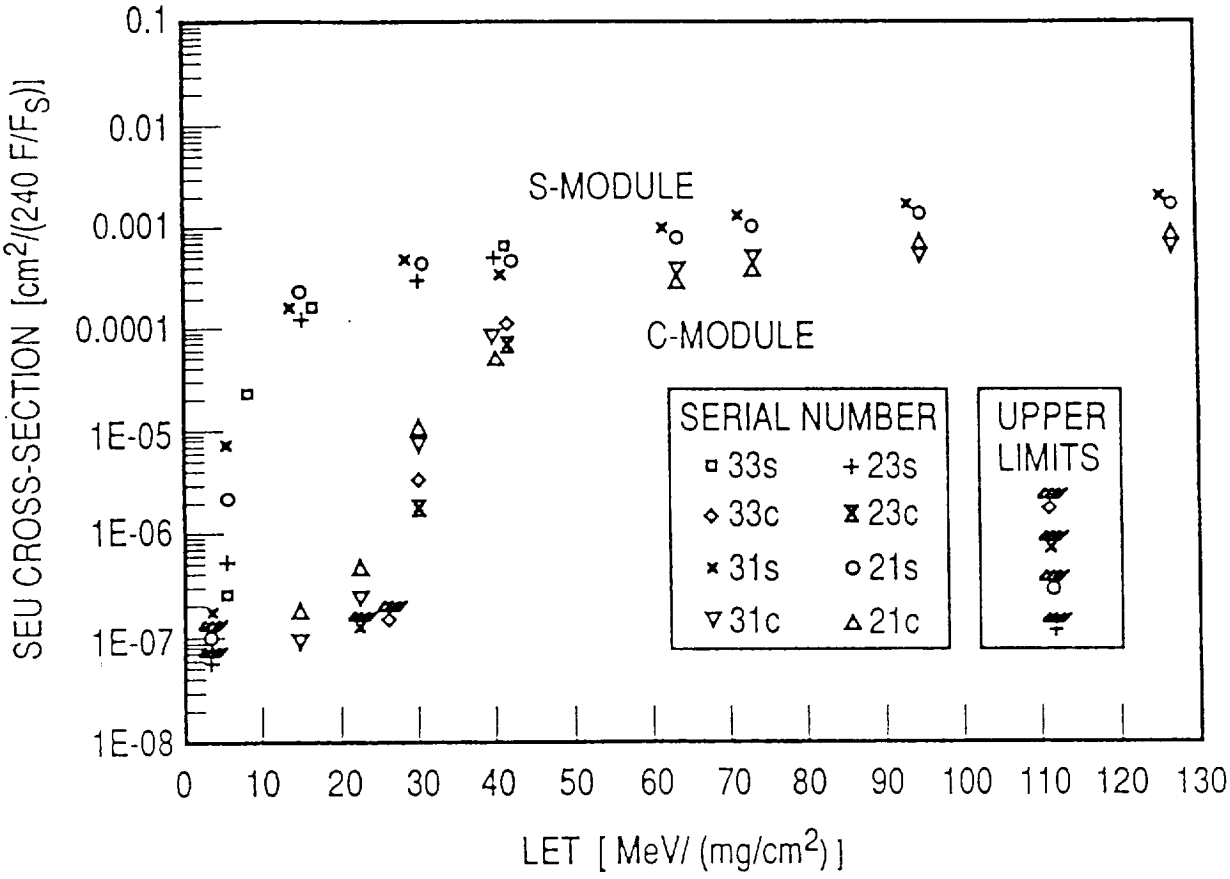


Figure 3. SEU Test Results for A1280

SECTION 3.3
DPA Product Analysis/Step Coverage

PARTS INFORMATION PROGRAM

ELECTRONIC PARTS RELIABILITY SECTION

PIP No. 305

JPL
Jet Propulsion Laboratory
California Institute of Technology

DATE 13 April 1992

SUBJECT:

Preliminary Product Analysis (PA) of ACT-21280B (1.2 μm) CMOS Field Programmable Gate Array (FPGA) Si-chip manufactured by Actel Corp.

SUMMARY:

Two ACT-21280B Si-chip samples (lot #UH-01, PC #18340) were submitted to the JPL LSI Group for destructive product analysis. This PA effort is a part of the JPL/NASA Quality Assurance Program in support of selection and qualification of field programmable gate array CMOS devices considered for use in flight hardware systems for the Earth Observation System (EOS) and Cassini Missions.

The evaluation results provide initial insight into the quality of FPGA Chip materials structures, and particularly into the quality of metal step coverage of chip two-level (Si-Cu-doped aluminum) metal interconnections which are as follows:

1) SEM examination of laterally exposed metal-2 and metal-1 interconnections show clean metal line width patterns, and alignment of metal-2 to metal-1 contacts, and metal-2 step coverage thickness over intrametal dielectrics and metal-1, as shown in Figures 3a through 5a.

2) SEM examination of two cross-sectioned chip segments: Figures 8a through 13d show identified cross-sectioned structures of metal-2 and metal-1 with thickness definition and step coverage quality. Metal-2 nominal thickness is approximately 1.1 μm thick compared with metal-2 thin step coverage features in intrametal SiO_2 via sidewalls to metal-1 contacts, and metal-2 thinning step coverage over unplanarized Spin-on Oxide (SOG) and Low Temperature Oxide (LTO) steps of intrametal dielectric above metal-1 contacts. These steps vary from 0.18 μm to 0.35 μm in thickness, as shown in Figures 8a, 9a, 9d, 11d and 13c.

SOURCE OF INFORMATION:

JPL LSI Engineering Group, Section 514, S. Suszko.

FOR ADDITIONAL INFORMATION CONTACT: Stefan Suszko **EXT:** 4-1716 or 4-7709

APPROVED: Group Supervisor - LSI Engineering Group

Metal-1 nominal thickness is approximately 0.75 μm compared with thinning features of metal-1 step coverage in BPSG via cuts to poly and Si contacts, which vary from 0.16 μm to 0.26 μm, as shown in Figures 8d, 9d, 10a, 11d and 12d. FPGA cell with programmed (fused) poly through oxide/nitride/oxide (ONO) dielectric to Si is identified in Figures 10c and 10d.

3) Figures 6a through 7d show laterally exposed MOS-transistor cells with thin nitride film over poly gate patterns, field oxide and FPGA cells with programmable poly (after removal of two-level metal interconnections and interlevel dielectrics). Exposed contact patterns to poly and Si are outlined in thin nitride, and show good alignment to poly and in active areas of Si-cells.

CONCLUSIONS

Evaluation results of the Actel FPGA 21280B 1.2 μm Si-chip show evidence of metal-2 thinning in via step coverage to metal-1 contacts, and over unplanarized steps of intrametal dielectrics (SOG and LTO) above metal-1 contacts. Metal-2 nominal thickness of 1.1 μm is reduced to 0.2 μm, as shown in Figures 8d, 9a and 9d.

- Metal-1 thin step coverage is evidenced in BPSG aperture cuts to poly and Si contacts, from nominal 0.75 μm metal thickness to 0.15 μm, as shown in Figures 8d, 9d, 10a, 11d and 12d.

- The thickness quality of metal-2 and metal-1 step coverage does not meet acceptance criteria of MIL-STD-883C. However, reliability data calculations for current density requirements might pass this metal step coverage in contact vias according to MIL-STD-38510, as calculated by Mike Sandor of JPL (Ref: JPL IOM 514-F-038-92, Calculation of Current Density for Actel 2.0 μm and 1.2 μm FPGA Technology).

- The FPGA 21280B 1.2 μm Si chip is a fairly new product technology, just over a year old, and the reliability database is still evolving and minimal on this product line. For the electrical and environmental functionality of this FPGA device, see the manufacturer's data sheets, attached. For additional information, contact M. Davarpanah, JPL component specialist.

PROCEDURE

The evaluation was performed on two Si-chips in accordance with MIL-STD-883C, Methods for Microcircuits (where applicable). One Si-chip was backscribed and cleaved into four segments. Two chip segments were used for lateral selective exposure and removal of chip materials levels. The other two chip segments were prepared as cross-sectioned samples and examined for definition and identification of chip materials layers on Si, their interface integrity and thickness dimensions (see Table I).

A second Si-chip was used for lateral exposure of materials without backscribing and cleaving it into separate chip segments.

Optical and SEM examinations were performed prior to and after each level of chip materials exposure, and X-ray spectroscopic analysis was used for identification of chip materials composition.

OPTICAL AND SEM EXAMINATIONS:

Figures 1a through 13d are optical and SEM photo views, which together with captions provide representative examples of FPGA chip and chip exposed materials levels and structures, their interface integrity, and thickness dimensions.

Table I. Physical Dimensions of ACT-21280B Die and Die Structures

Die/Die Structures	Dimensions
1. Die material: (Si), and size	12 x 12.7 mm
2. Die passivation: Nitride on SiO_2	≅ 1.2 μm
3. Die metallization: Si-and cu-doped Aluminum two-level metal interconnect; metal-2 top, metal-1 bottom level.	
4. Metal-2 thickness	≅ 1.1 μm
5. Minimum metal-2 step coverage thickness	≅ 0.2 μm
6. Metal-1 thickness	≅ 0.75 μm
7. Minimum metal-1 step coverage thickness	≅ 0.15 μm
8. Minimum metal-2 line width	≅ 2.0 μm
9. Minimum metal-1 line width	≅ 2.0 μm
10. Intrametal dielectric (SOG on LTO) thickness	≅ 0.65 μm
11. BPSG thickness	≅ 0.7 μm
12. Thin nitride thickness (on field oxide)	≅ 800 Å
13. Gate poly thickness	≅ 0.35 μm
14. Field oxide thickness	≅ 0.75 μm
15. Contact diameter to poly and Si	≅ 1.6 μm
16. ONO thickness	≅ 0.1 μm

Note: The chip materials dimensions were derived from SEM photo figures using SEM calibration reference line and magnification factor.

OPTICAL PHOTO VIEWS OF ACTEL CMOS-PAL (1.2 μm) Si-CHIP AND MAGNIFIED CHIP CIRCUIT SEGMENTS WITH NITRIDE AND SiO_2 PASSIVATION OVER 2-LEVEL METAL INTERCONNECTIONS.

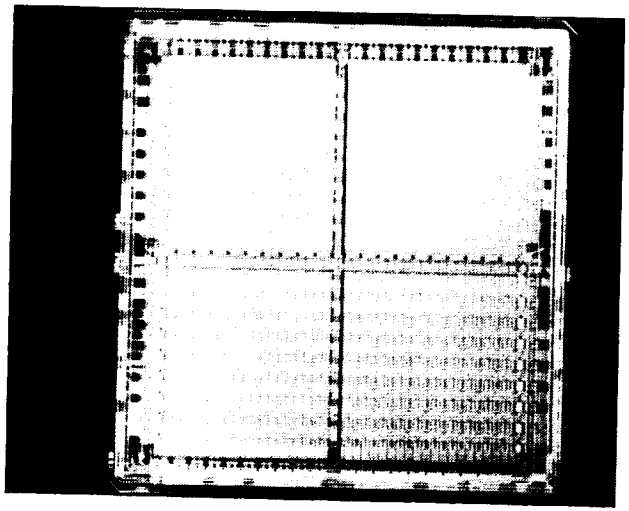


Figure 1a. 6X optical view of Actel PAL-chip (chip size 12 X 12.7 mm)

Figure 1b. 100X view of PAL-chip segment with chip logo and date.

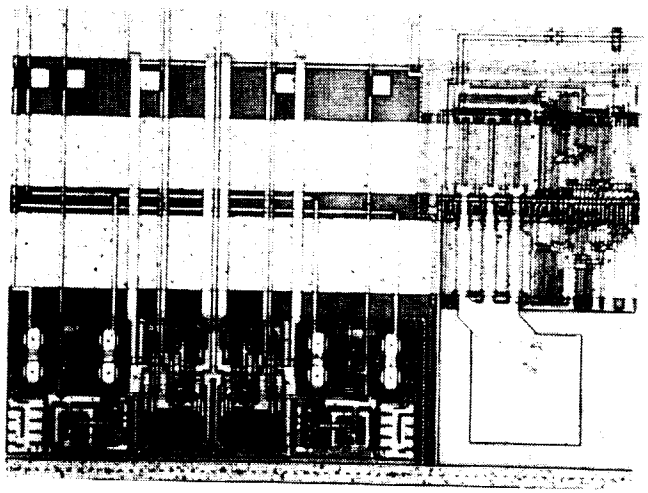


Figure 1c. 200X view of chip circuit segment with two-level metal interconnect.

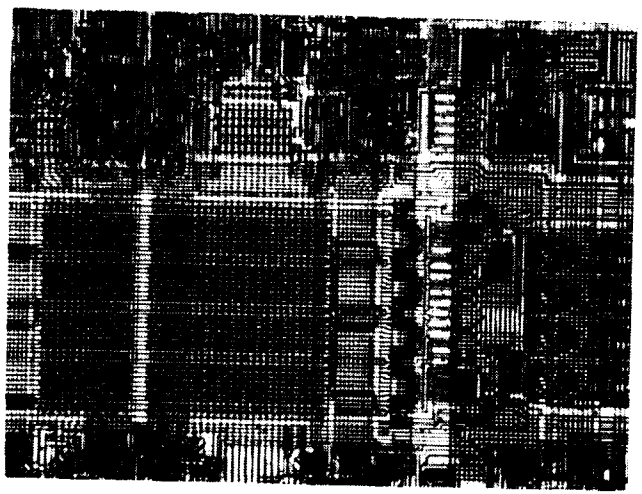


Figure 1d. 200X view of chip segment with PAL circuit pattern.

OPTICAL PHOTO VIEWS OF CMOS-PAL CHIP CIRCUIT SEGMENTS WITH NITRIDE AND SiO_2 PASSIVATION OVER 2-LEVEL METAL INTERCONNECTIONS.

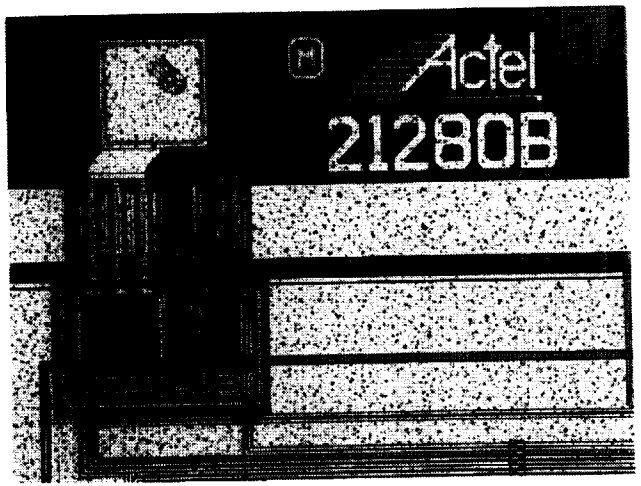


Figure 2a. 200X optical view of chip logo and output buffer with metal interconnections.

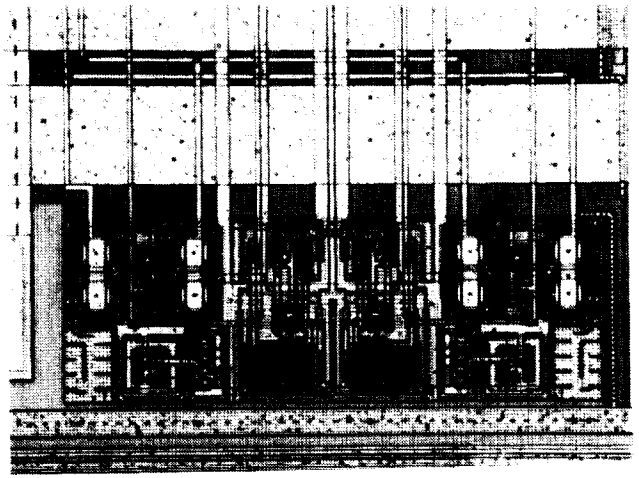


Figure 2b. 300X optical view of chip circuit with two-level metal interconnect pattern.

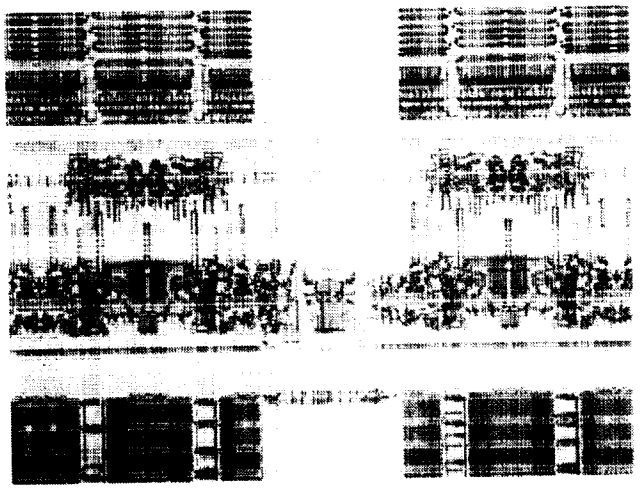


Figure 2c. 100X view of chip PAL circuit segment.

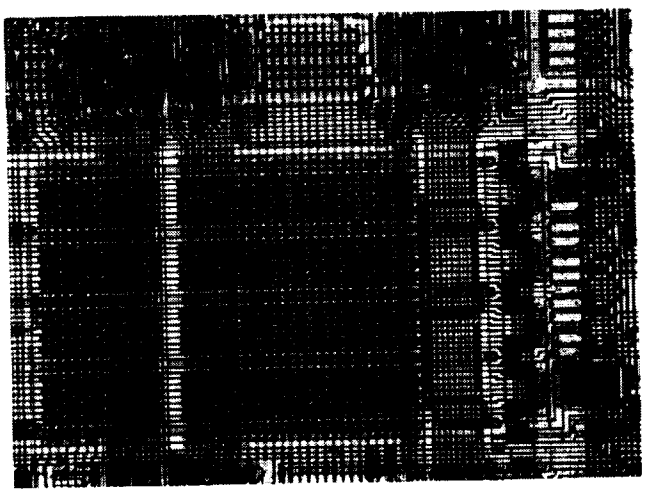


Figure 2d. 250X optical view of chip programmable logic array (PAL) segment with metal interconnections.

SEM PHOTO VIEW OF PAL CHIP SEGMENT WITH NITRIDE AND SiO_2 PASSIVATION.

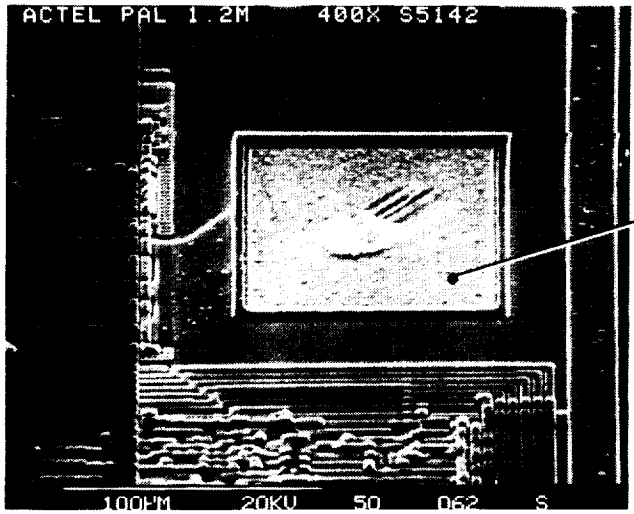


Figure 2e. 400X view of chip metal pad.

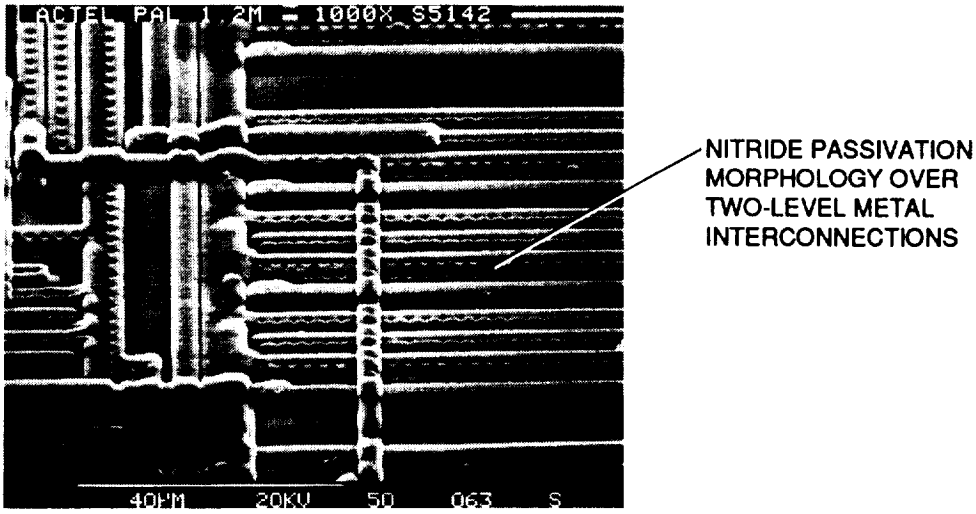


Figure 2f. 1000X SEM view of chip segment with nitride passivation morphology over two-level metal interconnections.

SEM PHOTO VIEWS OF PAL CHIP EXPOSED 2-LEVEL METAL INTERCONNECTIONS WITH METAL-2 TO METAL-1 CONTACTS AND STEP COVERAGE FEATURES (TOP NITRIDE AND SiO_2 PASSIVATION REMOVED).

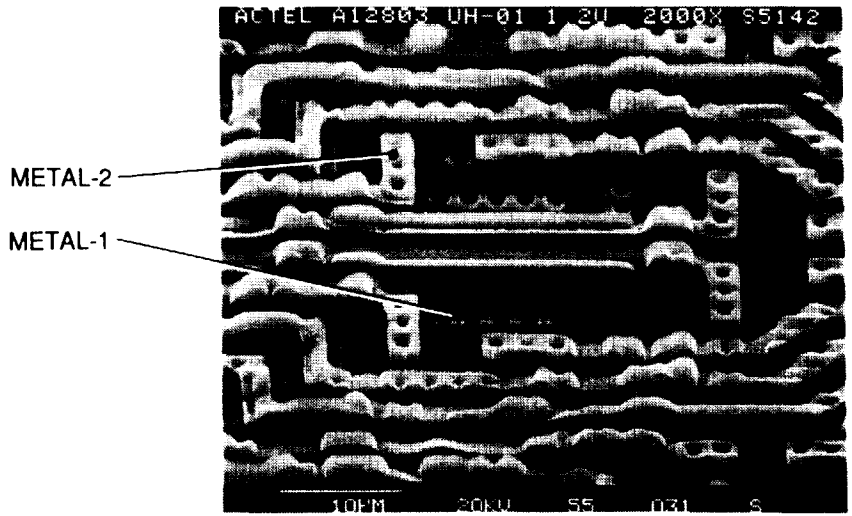


Figure 3a. 2kX side view of top metal-2 with contacts to metal-1.

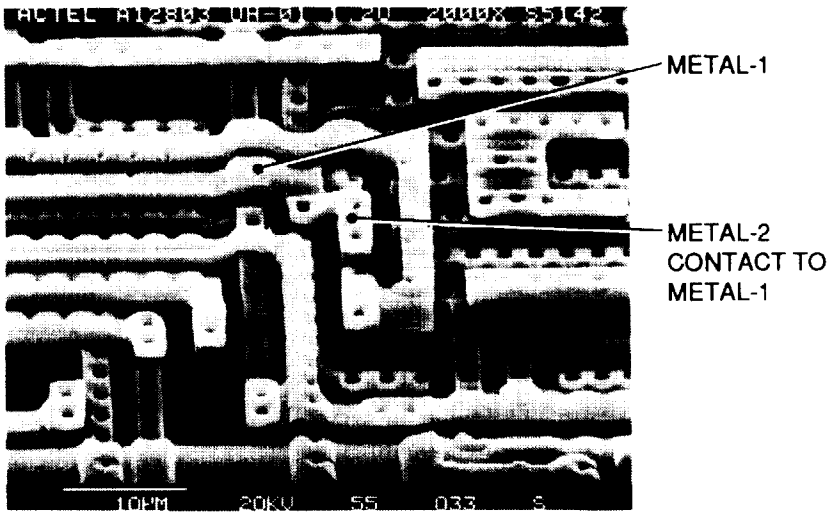


Figure 3b. 2kX side view of exposed top metal-2 with contacts to metal-1.

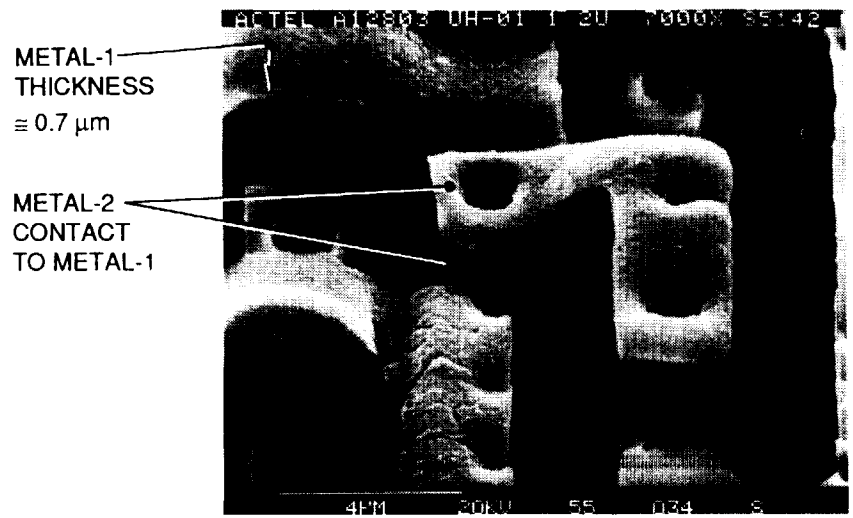


Figure 3c. 7kX side view of exposed metal-2 step coverage and contact features.

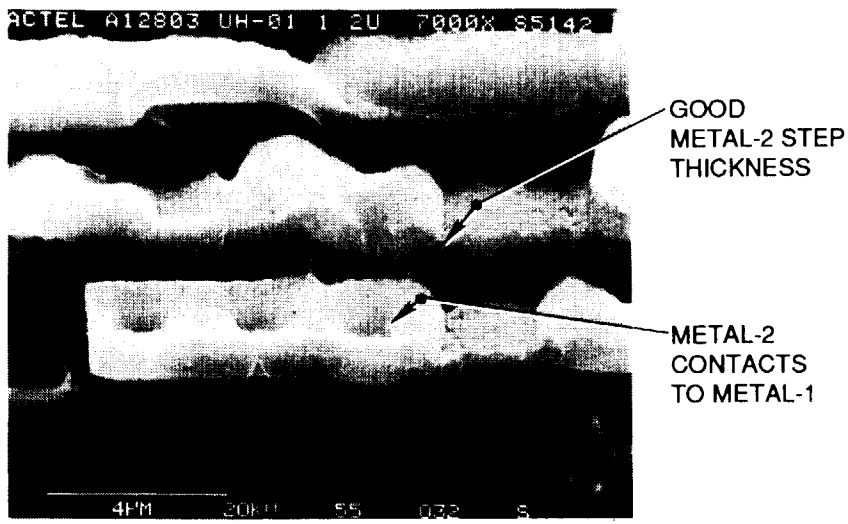


Figure 3d. 7kX side view of exposed metal-2 step coverage thickness over SiO_2 and metal-1 steps.

SEM PHOTO VIEWS OF PAL CHIP EXPOSED 2-LEVEL METAL INTERCONNECTIONS WITH STEP COVERAGE PATTERN OF METAL-2 OVER SiO_2 STEPS AND METAL-1 (TOP NITRIDE AND SiO_2 PASSIVATION REMOVED).

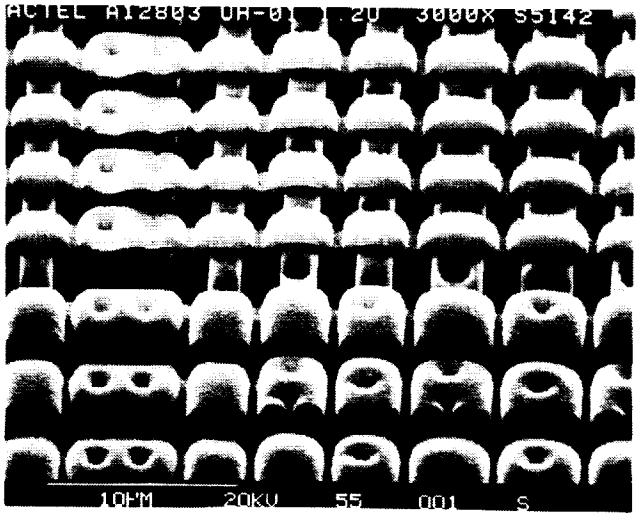


Figure 4a. 3kX side view of exposed top metal-2 step coverage features over SiO_2 and metal-1 steps.

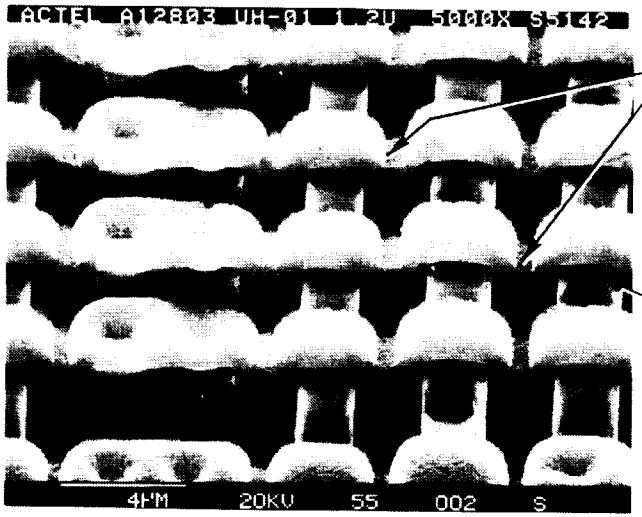


Figure 4b. 5kX side view of exposed top metal-2 step coverage over SiO_2 and metal-1 steps.

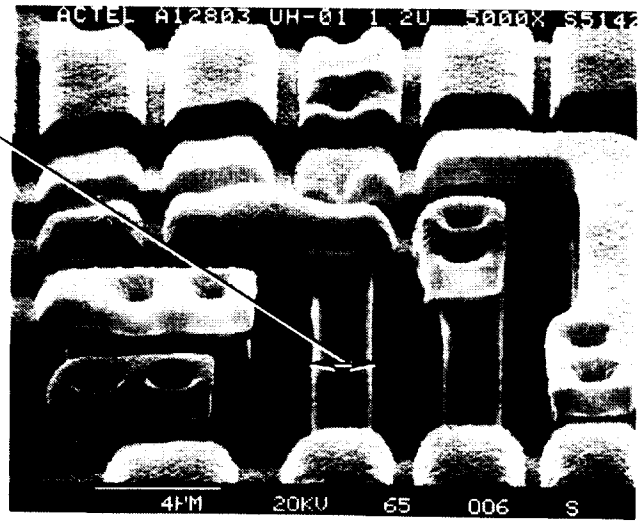


Figure 4c. 5kX side view of exposed metal-2 with contacts to metal-1.

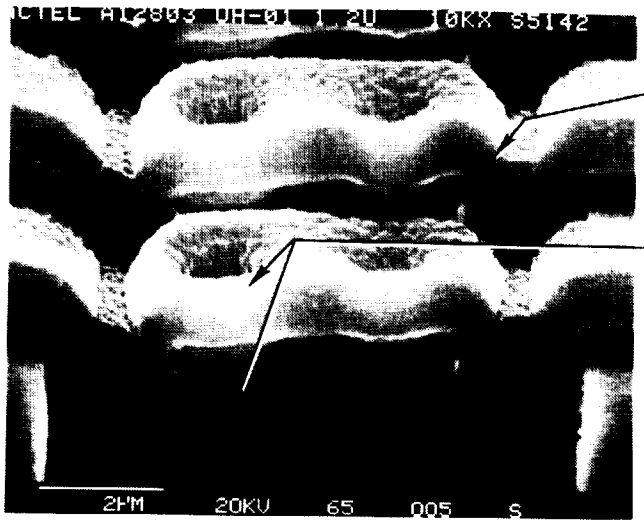


Figure 4d. 10kX side view of exposed metal-2 with contacts and step coverage thickness, and metal-1 thickness.

SEM PHOTO VIEWS OF EXPOSED METAL-2 STEP COVERAGE FEATURES AND LINE WIDTH PATTERNS.

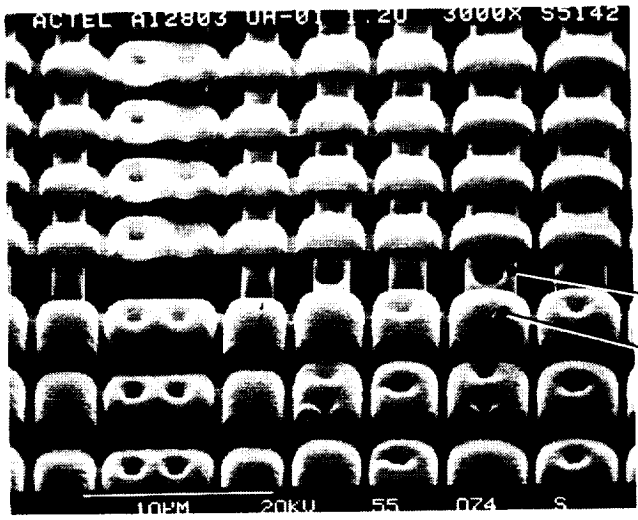


Figure 5a.
3kX side view of exposed metal-2 step coverage features over SiO_2 and metal-1 steps.

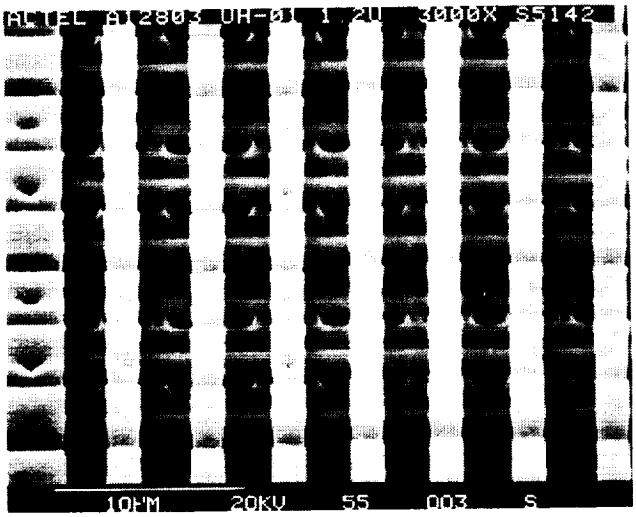


Figure 5b.
3kX view of exposed metal-2 line width patterns and separation.

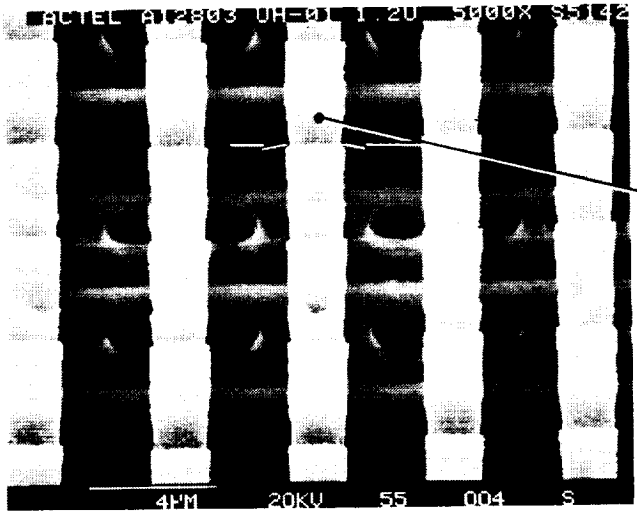


Figure 5c.
5kX view of metal-2 line widths.

SEM PHOTO VIEWS OF EXPOSED CONTACTS TO POLY GATES, AND PROGRAMMABLE POLY ARRAY LOGIC (PAL) BLOCKS (METAL-2 AND METAL-1, AND INTRAMETAL DIELECTRICS REMOVED).

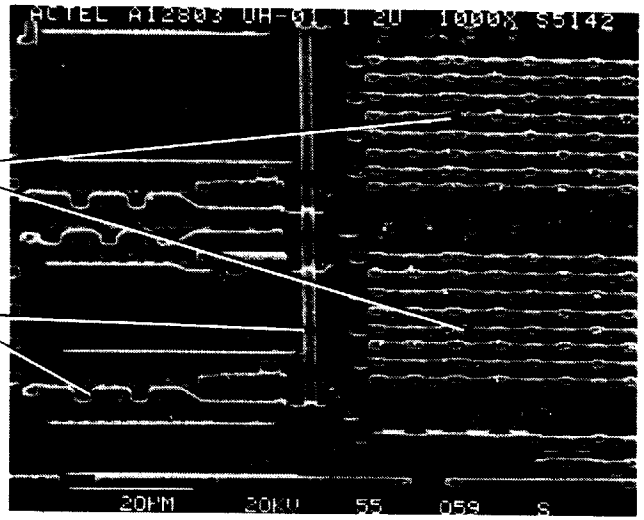


Figure 6a. 1kX side view of exposed contacts to poly gates and (PAL) programmable poly pattern with thin nitride.

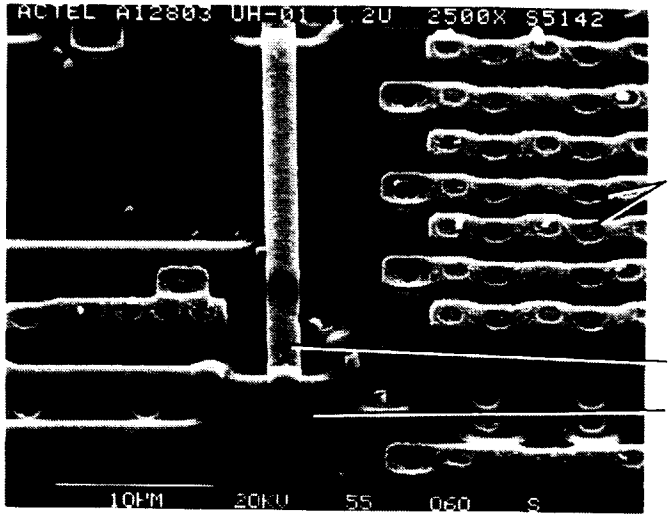


Figure 6b. 2.5kX side view of exposed thin nitride over poly gates and PAL poly.

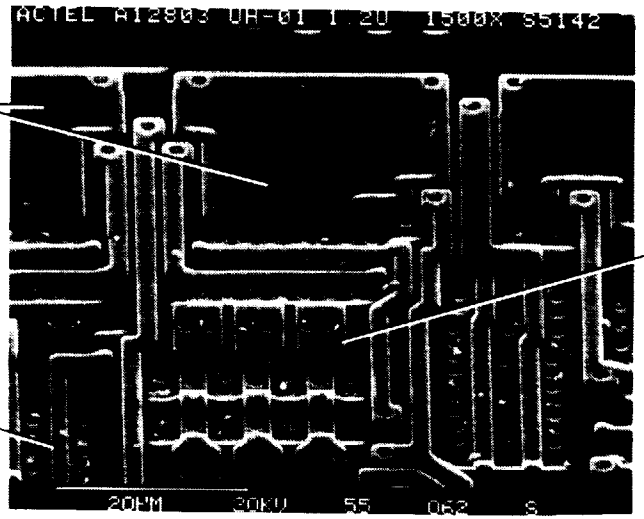


Figure 6c. 1.5kX side view of poly-capacitor plates, gate poly and (PAL) poly.

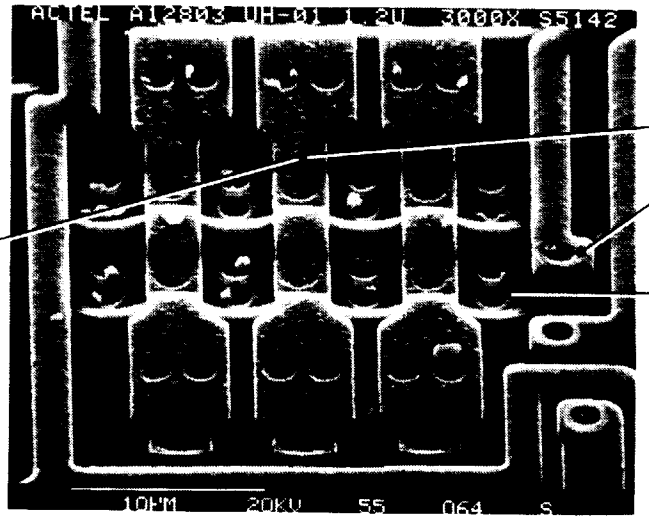


Figure 6d. 3kX side view of PAL poly with programmable contacts to Si, and gate poly contacts on field oxide.

SEM PHOTO VIEWS OF EXPOSED CONTACTS TO POLY GATES, AND (PAL) PROGRAMMABLE POLY TO Si (METAL-2, METAL-1 AND INTRAMETAL DIELECTRICS REMOVED).

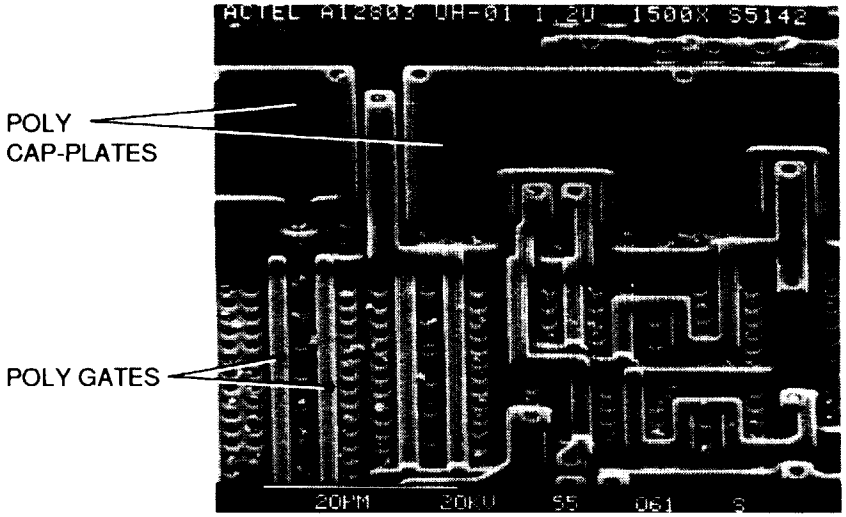


Figure 7a. 1.5kX side view of exposed contacts to poly gate patterns and to Si.

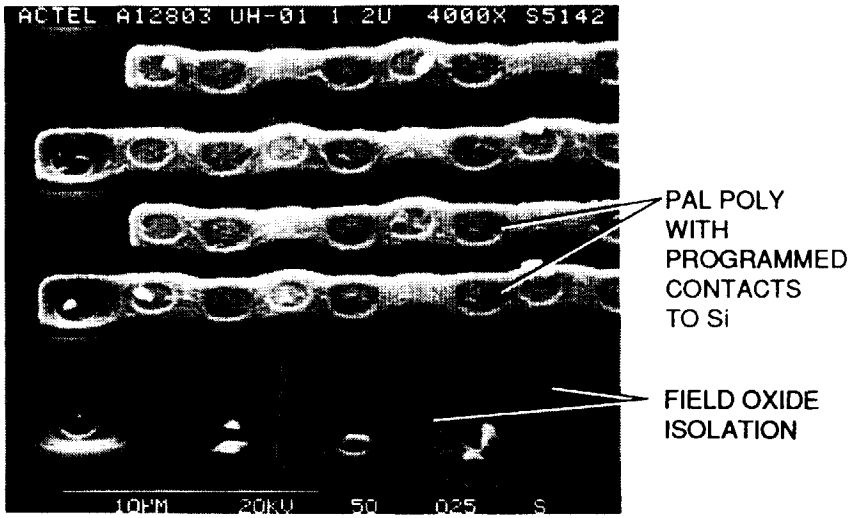


Figure 7b. 4kX side view of (PAL) programmable poly with programmed interface to Si.

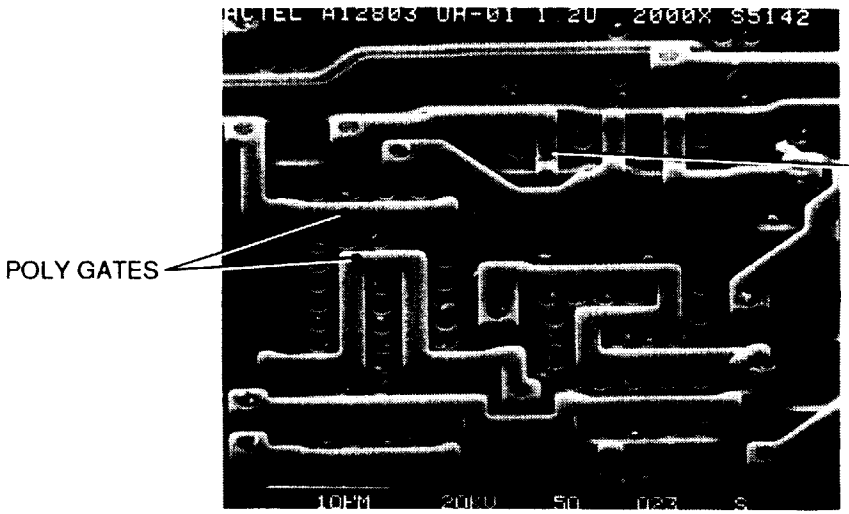


Figure 7c. 2kX side view of exposed MOS transistor cells and gate patterns, and Si contacts.

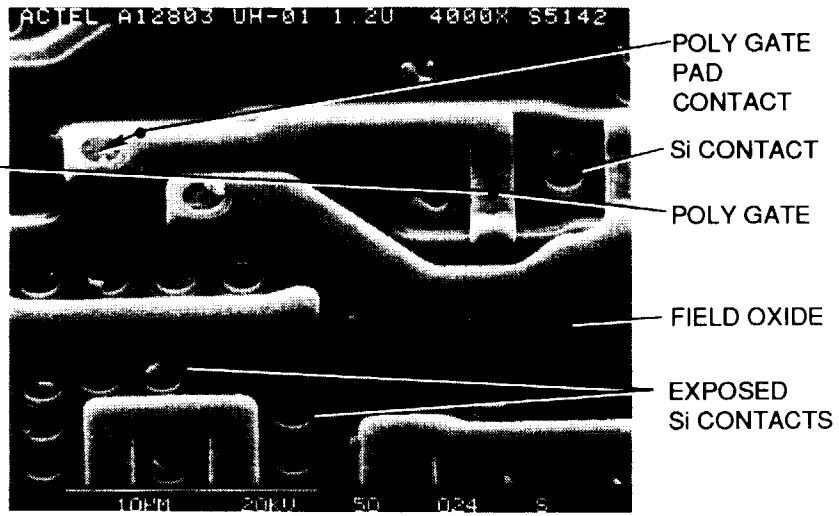


Figure 7d. 4kX side view of exposed contacts to poly gate pads on thick field oxide, and Si contacts.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE PATTERNS, ON Si SUBSTRATE.

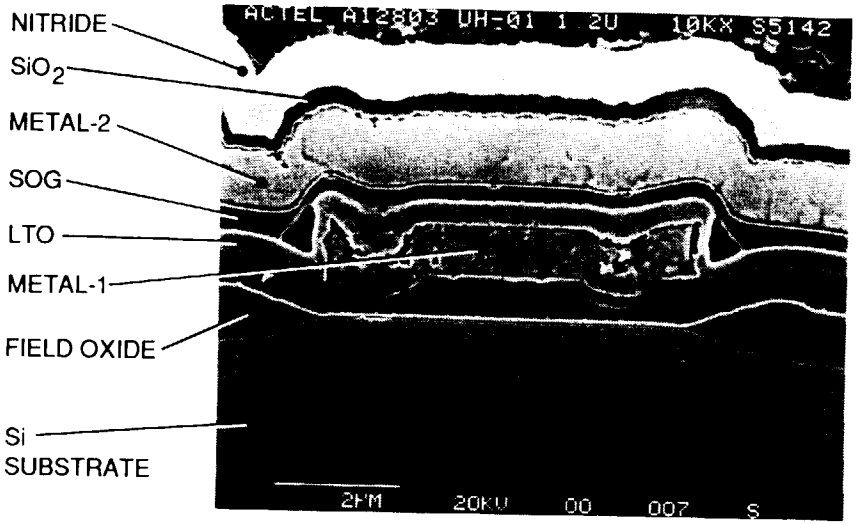


Figure 8a. 10kX view of top 2-level nitride and SiO_2 passivation over 2-level (Si-Cu doped) Al metal.

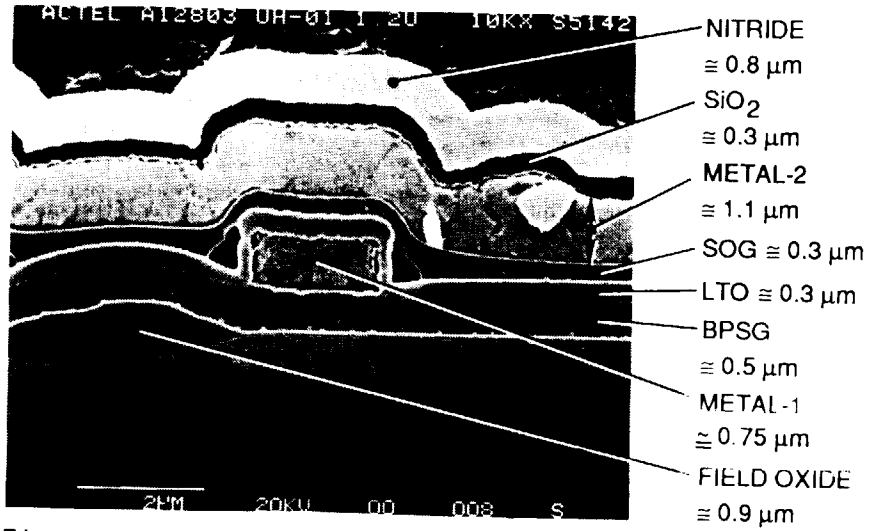


Figure 8b. 10kX view of top metal-2 step over SOG and LTO and metal-1 line width on BPSG, and thickness.

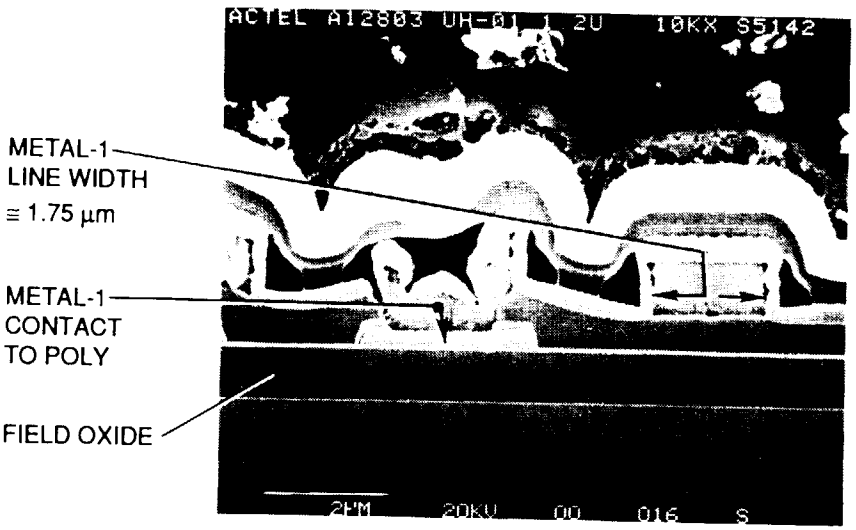


Figure 8c. 10kX view of metal-1 line, and contact to poly pad on thick field oxide.

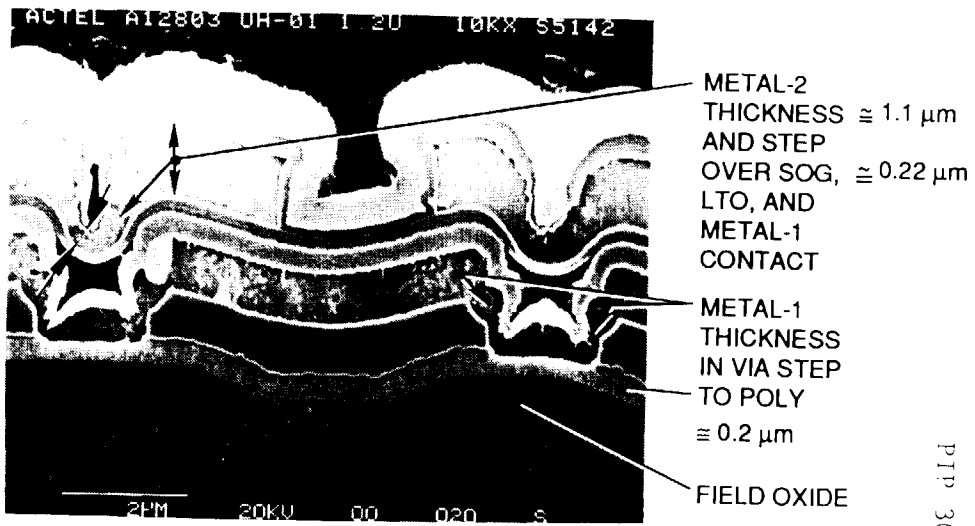


Figure 8d. 10kX view of metal-2 step features over SOG and LTO and metal-1 contacts to poly and step thickness.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE PATTERNS, ON SI-SUBSTRATE.

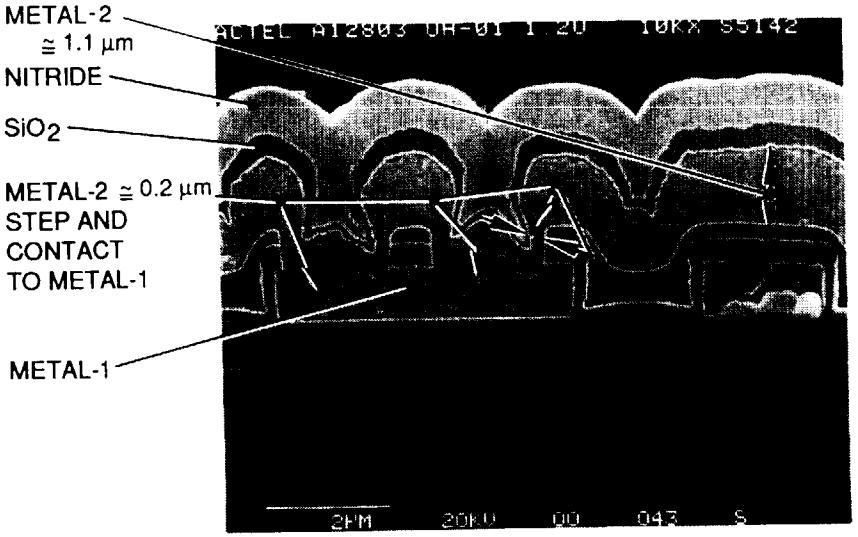


Figure 9a. 10kX view of metal-2 dual contacts to metal-1, and metal-1 line width and thickness.

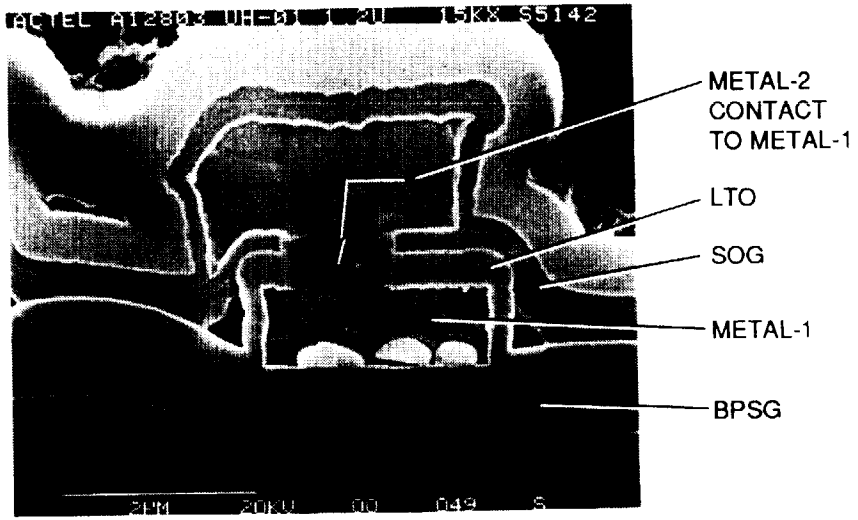


Figure 9b. 15kX view of metal-2 contact features to metal-1.

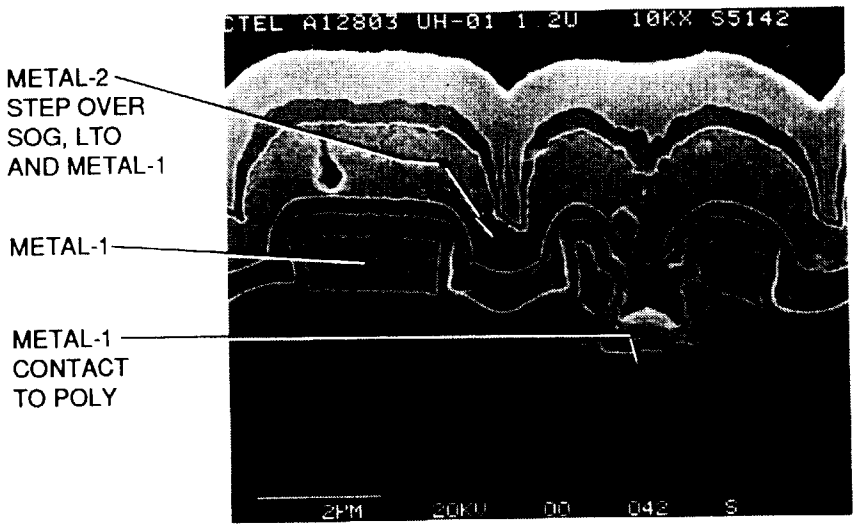


Figure 9c. 10kX view of metal-2 steps over SOG and LTO and metal-1, and metal-1 contact to poly.

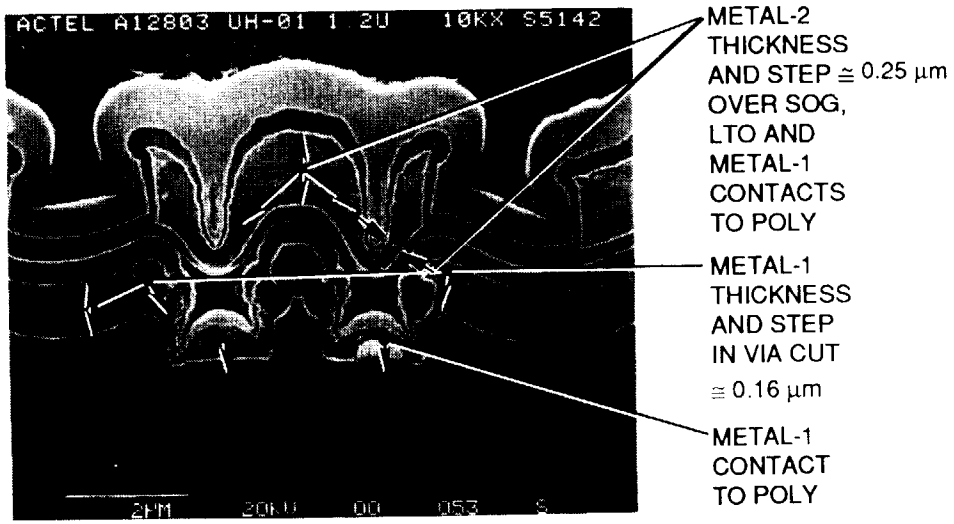


Figure 9d. 10kX view of metal-2 step features over SOG and LTO and metal-1 contacts to poly, and metal-1 via step coverage.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR THICKNESS AND INTERFACE INTEGRITY ON Si SUBSTRATE.

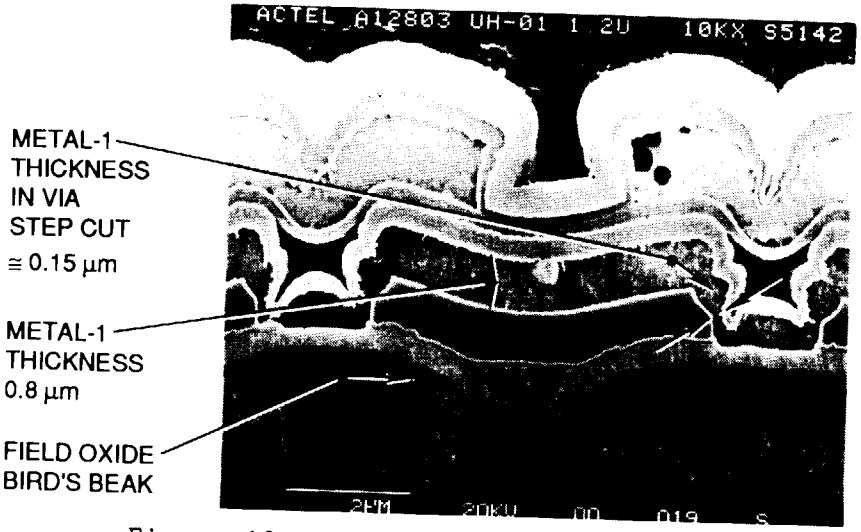


Figure 10a. 10kX view of metal-1 contacts and via step coverage to poly.

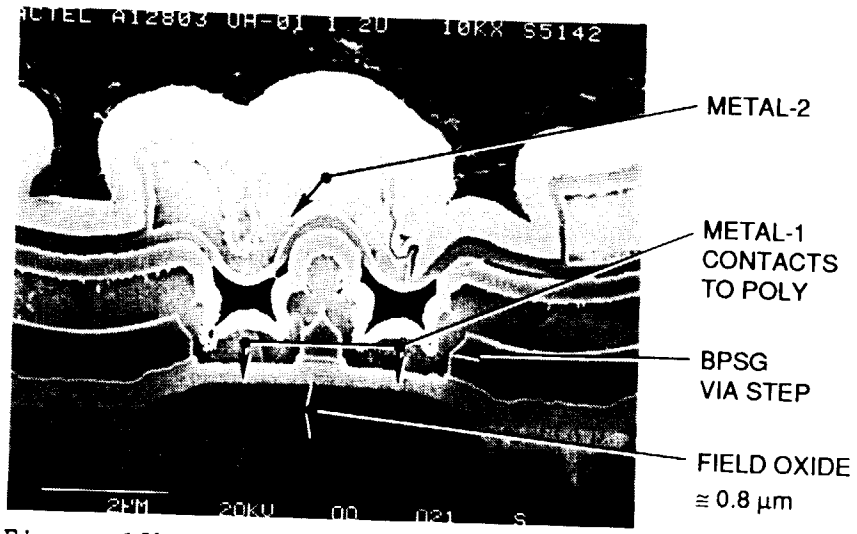


Figure 10b. 10kX view of metal-1 twin metal contacts to poly, and metal-1 thickness in BPSG via step.

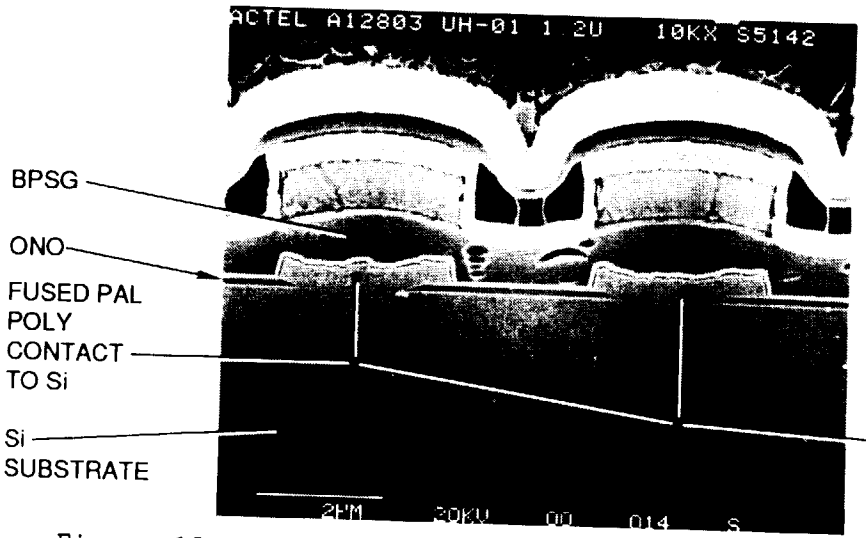


Figure 10c. 10kX view of PAL poly programmable contacts to Si through oxide/ nitride/oxide (ONO) dielectric.

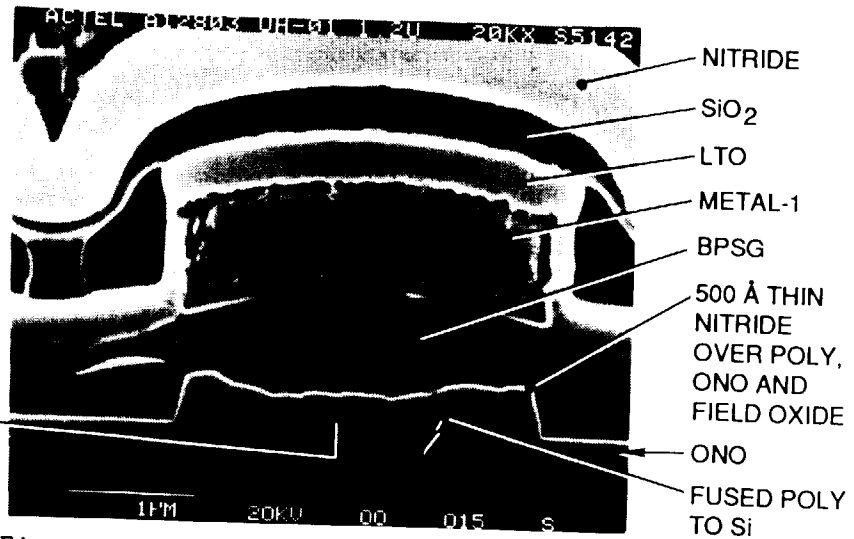


Figure 10d. 20kX view of programmed poly (fused) to Si on oxide/nitride/ oxide (ONO) dielectric.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS, THEIR INTERFACE INTEGRITY AND THICKNESS DIMENSIONS.

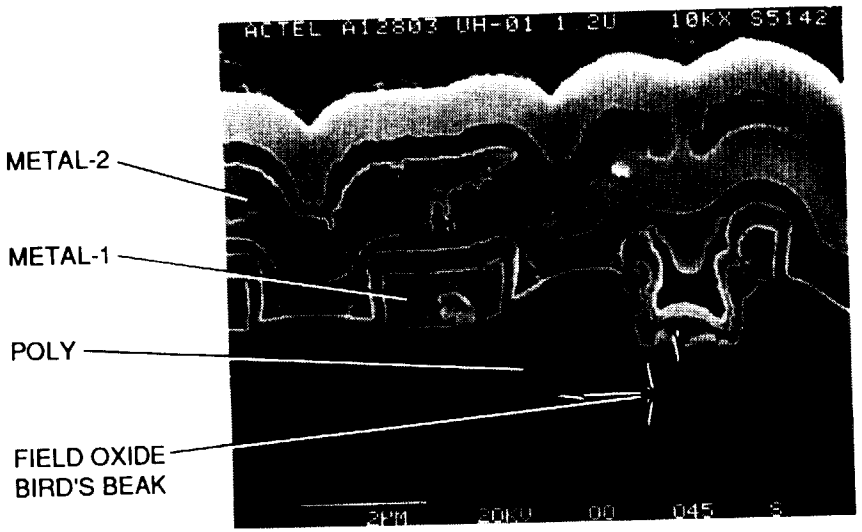


Figure 11a. 10kX view of metal-1 contact to poly, and metal thickness in via step cut.

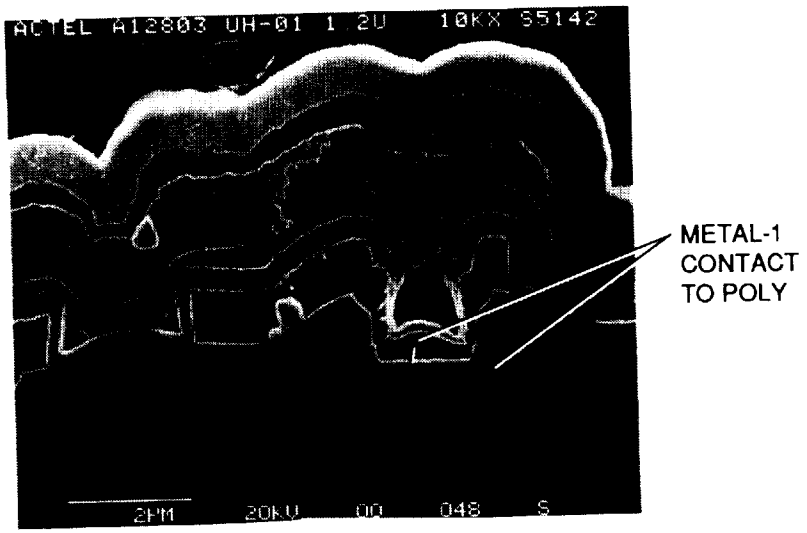


Figure 11b. 10kX view of metal-1 contact to poly, and metal thickness in via step cut.

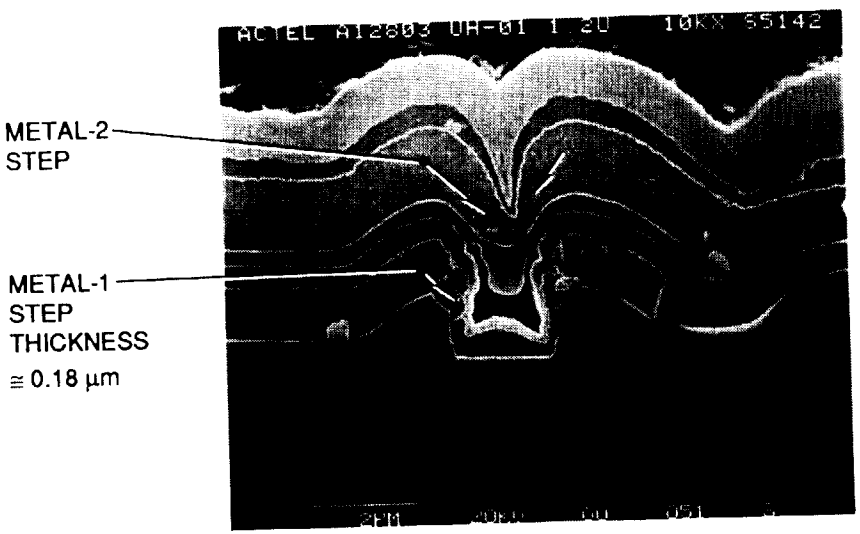


Figure 11c. 10kX view of metal-2 step over SOG and LTO and metal-1 contact to poly pad on thick field oxide.

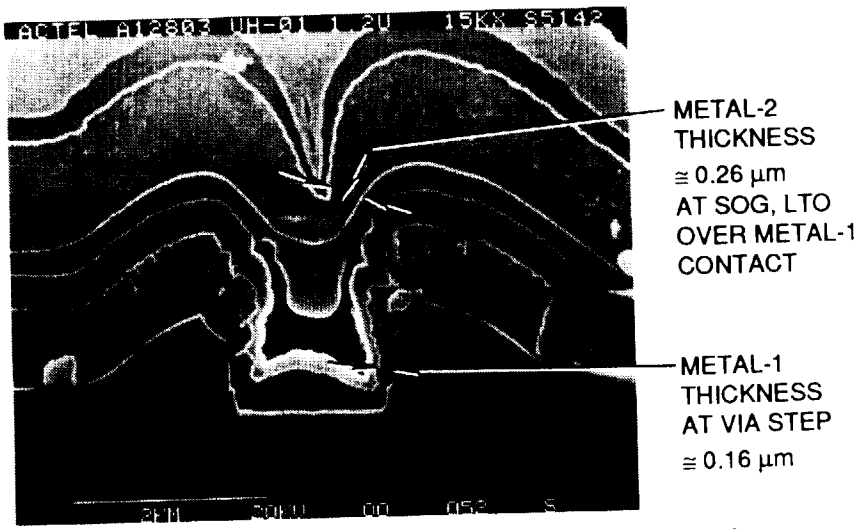


Figure 11d. 15kX view of metal-2 step, and metal-1 contact to poly with metal thickness in via step cut.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS SHOWING METAL-2 CONTACTS TO METAL-1, AND METAL-1 TO Si CONTACTS, AND METAL THICKNESS COVERAGE IN VIA STEP CUTS

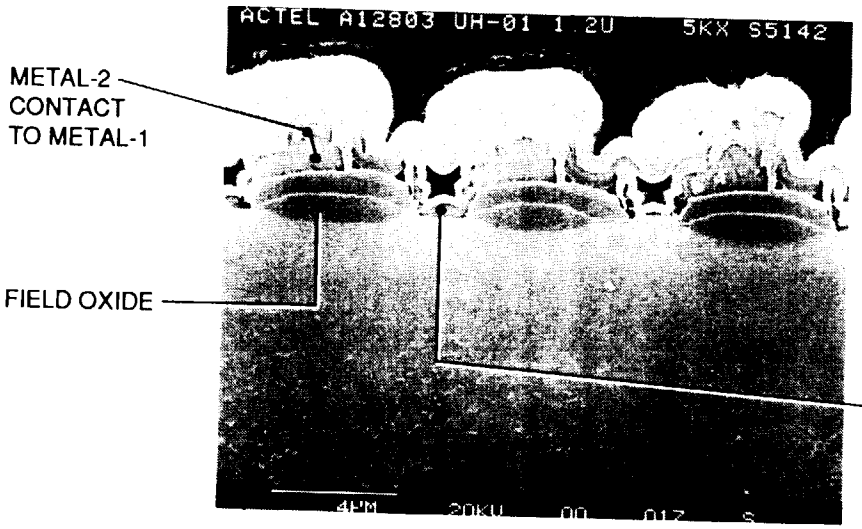


Figure 12a. 5kX view of metal-2 contacts to metal-1 and metal-1 contact to Si.

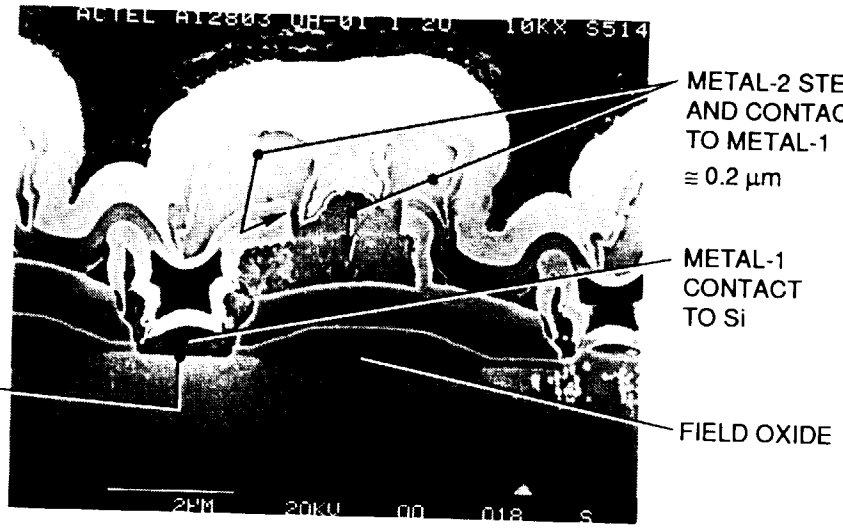


Figure 12b. 10kX view of metal-2 contact to metal-1, and metal-1 contact to Si with metal step coverage thickness in via step cut.

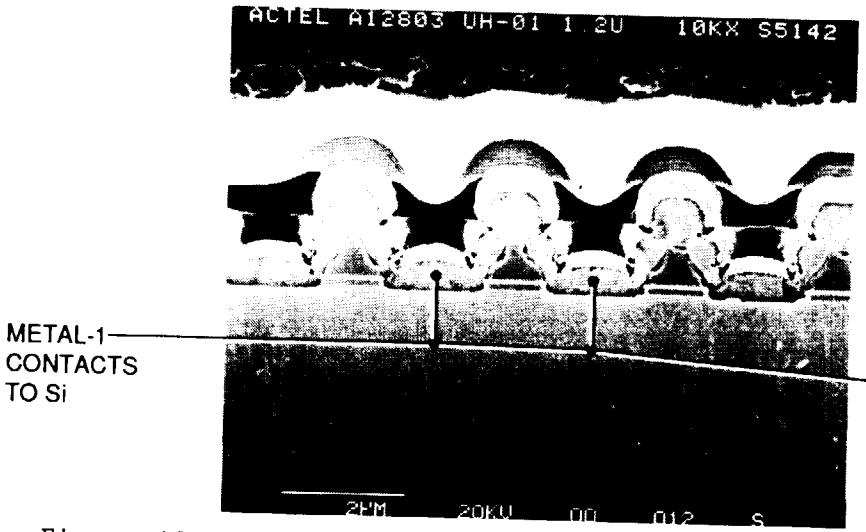


Figure 12c. 10kX view of metal-1 contacts to Si and metal thickness features in via step cuts.

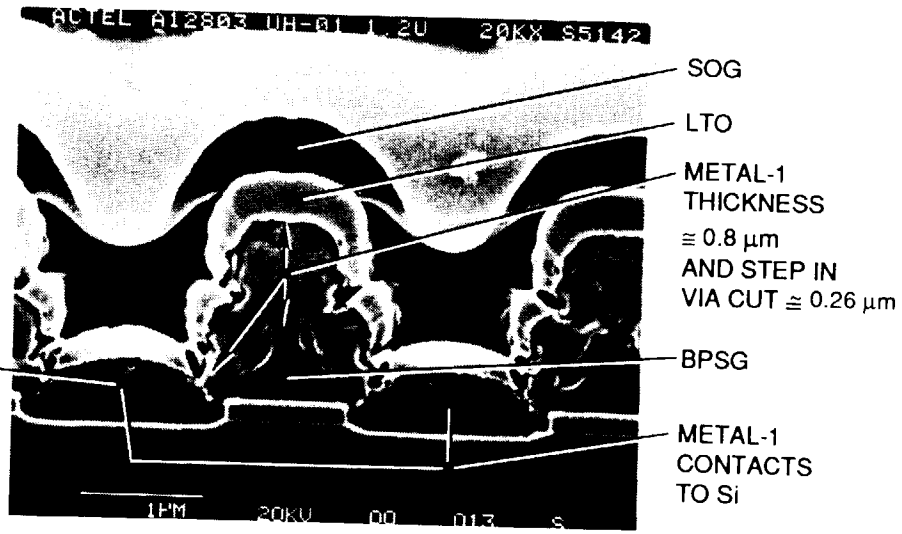


Figure 12d. 20kX view of metal-1 contacts and step coverage thickness in via step cuts.

SEM PHOTO VIEWS OF PAL CHIP CROSS-SECTIONED MATERIALS ON SI SUBSTRATE.

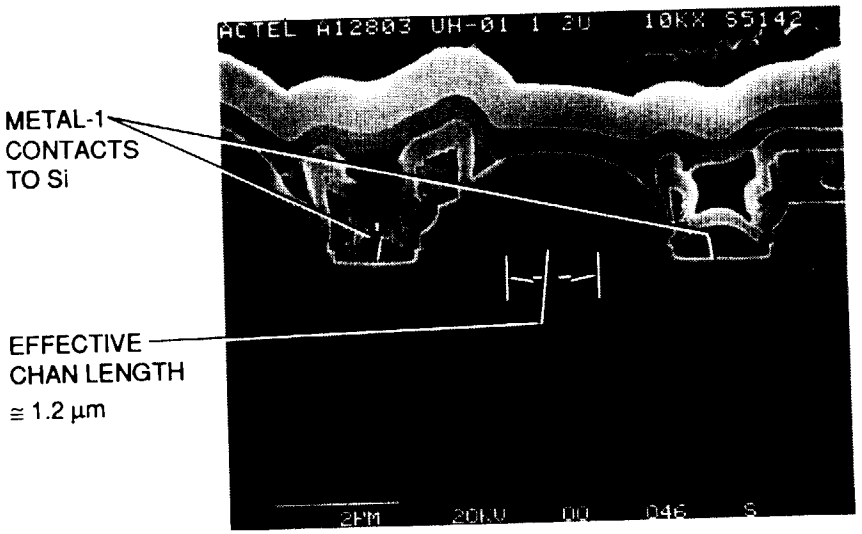


Figure 13a. 10kX view of poly gate length and effective channel length.

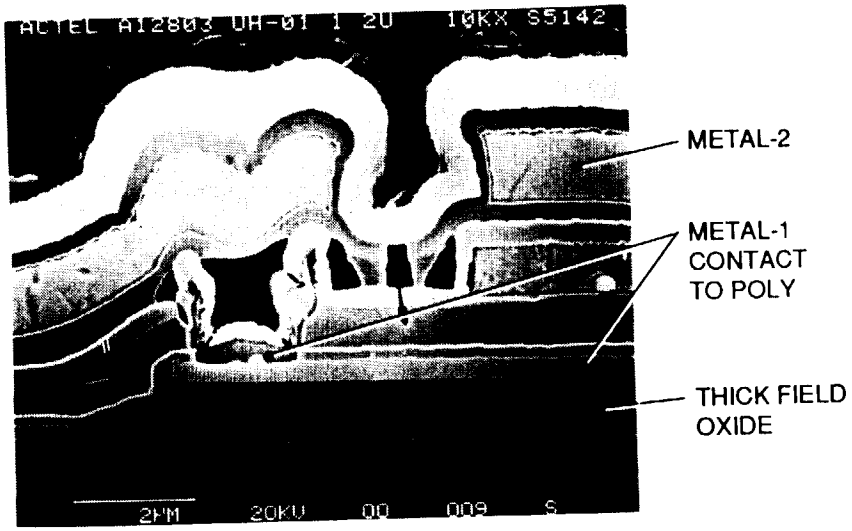


Figure 13b. 10kX view of metal-1 contact features to poly on thick field oxide.

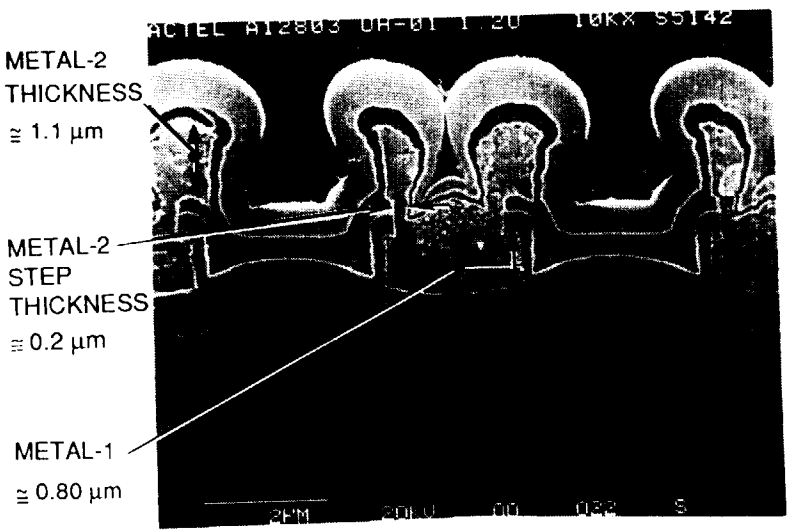


Figure 13c. 10kX view of metal-2 contact to metal-1 with metal-2 step thickness in SiO_2 via step.

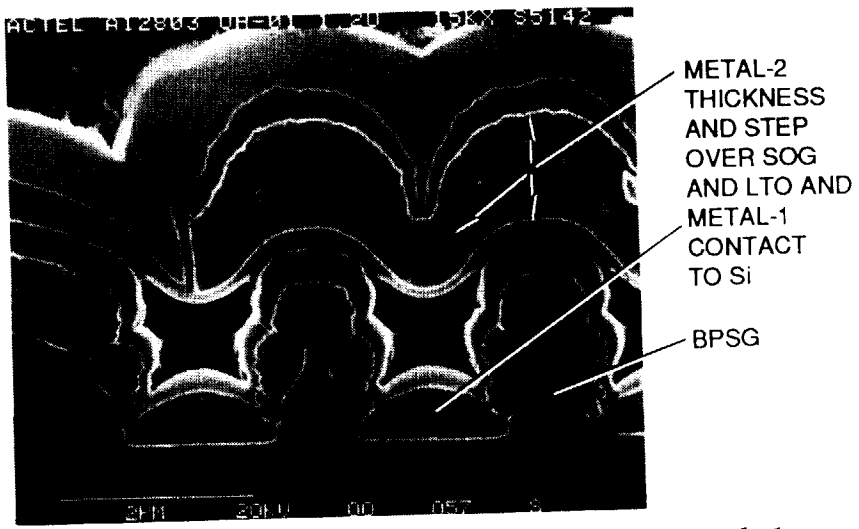


Figure 13d. 15kX view of metal-2, and metal-1 contacts with step coverage features in via step cuts.

ACT™ 2 Field Programmable Gate Arrays

Features

- Up to 8000 Gate Array Gates (20,000 PLD/LCA™ equivalent gates)
- Replace up to 210 TTL Packages
- Replace up to 69 20-Pin PAL Packages
- Design Library with over 250 Macros
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- 16-Bit Counter Performance to 85 MHz
- 16-Bit Accumulator Performance to 33 MHz
- Flip-Flop Toggle Rates to 120 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable

Product Family Profile

Device	A1280	A1240	A1225
Capacity			
Gate Array Equivalent Gates	8,000	4,000	2,500
PLD/LCA Equivalent Gates	20,000	10,000	6,250
TTL Equivalent Packages	210	105	70
20-Pin PAL Equivalent Packages	69	34	23
Logic Modules	1,232	684	451
S-Modules	624	348	231
C-Modules	608	336	220
Flip-Flops (maximum)	998	565	382
Routing Resources			
Horizontal Tracks/Channel	36	36	36
Vertical Tracks/Column	15	15	15
PLICE® Antifuse Elements	750,000	400,000	250,000
User I/Os (maximum)	140	104	83
Packages[1]	176 CPGA 160 PQFP	132 CPGA 144 PQFP	100 CPGA 100 PQFP 84 PLCC
Performance[2]			
16-Bit Counters	55 MHz	75 MHz	85 MHz
16-Bit Accumulators	30 MHz	33 MHz	33 MHz
CMOS Process	1.2 µm	1.2 µm	1.2 µm

Note:
1. See product plan on page 4 for package availability.
2. Performance is based on a -1 speed graded device at commercial worst-case operating conditions.

Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays. The ACT 2 family presents a two-module architecture, consisting of C-Modules and S-Modules. These modules are optimized for both combinatorial and sequential designs (see Figure 1). Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining upward compatibility with the ACT 1 design environment. The devices are implemented in silicon gate, 1.2-µm, two-level metal CMOS, and employ Actel's PLICE antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance and fast time-to-production through user programming. The ACT 2 family is supported by the Action Logic™ System (ALS), which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is supported on the following platforms: 386/486 PC, and Sun®, HP® and Apollo® workstations. It provides CAE interfaces to the following design environments: Valid™, Viewlogic®, Mentor Graphics®, HP DCS and OrCAD™.

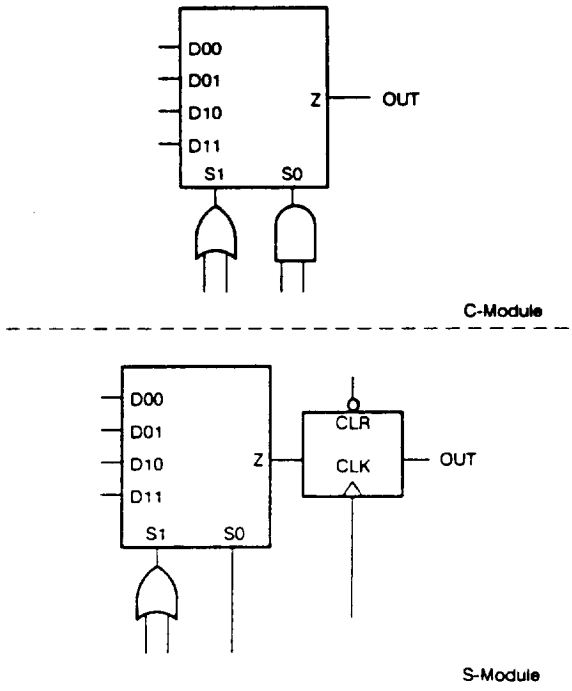


Figure 1. ACT 2 Two-Module Architecture

ACT 2 Architecture

Routing efficiency with large gate count devices is improved by increased routing resources and antifuse programming elements, as well as architectural enhancements. Horizontal routing tracks/channel are increased to 36 (vs. 25 for ACT 1); vertical routing tracks/column are increased to 15 (vs. 13 for ACT 1). All speed-critical module-to-module connections are accomplished with only two low-resistance antifuse elements. Most connections are implemented with either two or three antifuse elements (see Figure 2). No connections are allowed with more than four antifuse elements in the path. This results in fully automatic placement and routing. This device utilization is typically 85% to 95% of available logic modules and 80% of total gates.

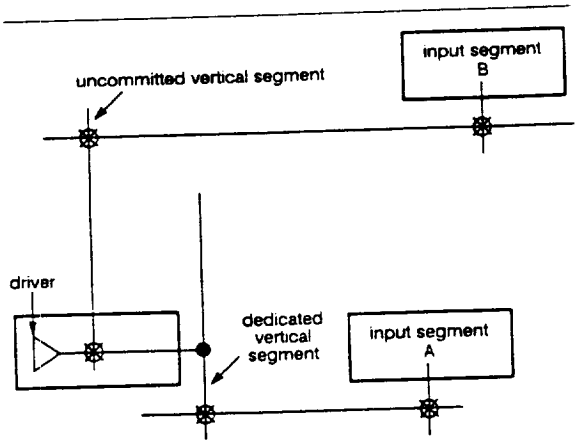


Figure 2. ACT 2 Routing Architecture

Two Module Design: C-Modules and S-Modules

The ACT 2 family has dedicated combinatorial and combinatorial-sequential modules (see Figures 3 and 4). The combinatorial module, *C-Module*, has been enhanced to implement high fan-in combinatorial macros, such as 5-input AND, OR, NAND and NOR gates. In addition, AND-OR gates, AND-XOR gates, XOR gates and many other combinatorial functions are available.

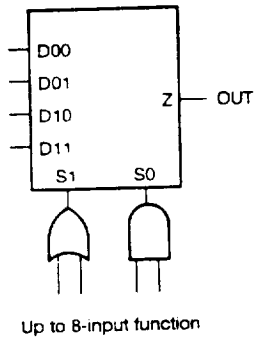


Figure 3. C-Module Implementation

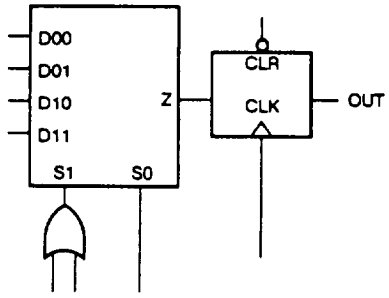
The combinatorial-sequential module, *S-Module*, is optimized to implement high-speed flip-flops within a single module. In addition, they include combinatorial logic within the S-Module, which allows an additional level of logic to be implemented without any additional propagation delay. Actel's ALS software automatically combines the combinatorial and sequential logic into the S-Module.

Hard and Soft Macros

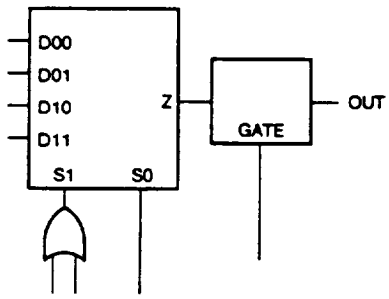
A building block approach is used for designing FPGAs within the Actel environment. Over 250 schematic representations of widely used logic functions are stored within the ACT 2 macro library. Each macro represents one of our basic to complex building blocks from which you may build your design. These macros include simple logic functions, such as AND gates, and more complex logic functions, such as 16-bit counters and accumulators.

These macros are implemented within the ACT 2 architecture by using one or more C-Modules and/or S-Modules. Over 150 of these macros are implemented within single modules, with an additional 25 macros implemented by connecting only two modules. One-module and two-module macros have a small propagation delay variance, which enables accurate performance prediction. These macros are called *hard macros*, and their propagation delays are specified within this datasheet. Combinable hard macros can be combined with the sequential logic within the S-Module.

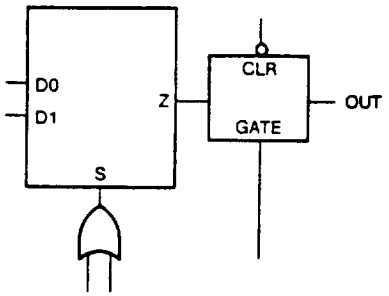
More complex logic functions are also included in the macro library. These *soft macros* are implemented by using several hard macros. The performance of soft macros depends on the application and is optimized by "criticality." Criticality is a method of easily defining the speed critical paths in a particular application.



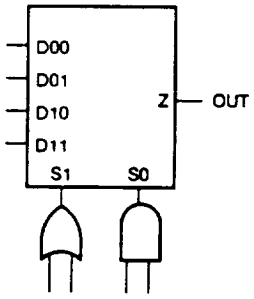
Up to 7-input function plus D-flip-flop with clear.



Up to 7-input function plus latch.



Up to 4-input function plus latch with clear.



Up to 8-input function (same as C-Module).

Figure 4. S-Module Implementations

Programmable I/O Pins

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Inputs are TTL and CMOS-compatible. Output drive levels meet 10 mA TTL and 6 mA HCT standards. Optional transparent latches at the I/O pins are provided for both inputs and outputs. I/O latches can be combined with latches in the array to implement master-slave flip-flops.

Low-Skew Clock Network

Two low-skew clock distribution networks are provided. Each network can be driven by either of two dedicated I/O pins or from internal logic. Clock skew is a function of the flip-flop distribution, and is guaranteed to be less than two nanoseconds in duration.

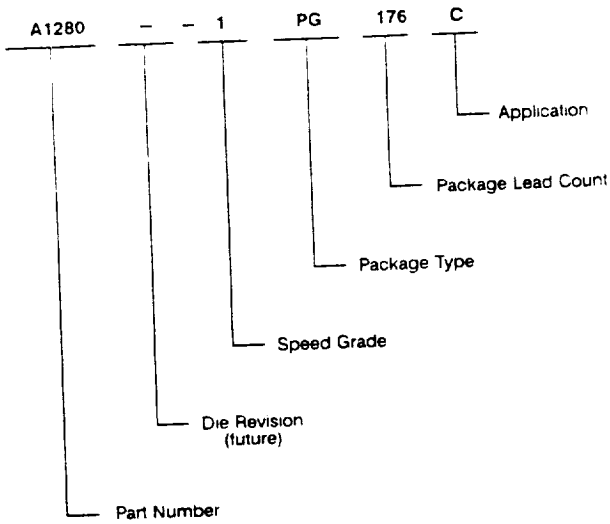
100% Tested Product

ACT 2 device functionality is fully tested before shipment and during device programming. Routing tracks, logic modules, and programming, debug, and test circuits are 100% tested before shipment. Antifuse integrity also is tested before shipment. Programming algorithms are tested when a device is programmed using Actel's Activator®2.

Probe Pins

ACT 2 family devices have two independent diagnostic probe pins, which allow the user to observe any two internal signals. Signals may be viewed on a logic analyzer using Actel's Actionprobe® diagnostic tools. The probe pins can be used as user-defined I/Os when debugging has been completed. After the design has been verified, the pins' probing capabilities can be terminated to protect the design's confidentiality.

Ordering Information



Product Plan

	Speed Grade		Application			
	Std	-1*	C	I	M	B
A1280 Device						
176-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	–	✓	P
160-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	–	–
A1240 Device						
132-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	–	✓	P
144-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	–	–
A1225 Device						
100-pin Ceramic Pin Grid Array (PG)	P	P	P	–	P	P
100-pin Plastic Quad Flatpack (PQ)	P	P	P	P	–	–
84-pin Plastic Leaded Chip Carrier (PL)	P	P	P	P	–	–

Applications: C = Commercial, I = Industrial, M = Military, B = 883B

Availability: ✓ = Available, P = Planned, – = Not Planned

* Speed Grade: -1 = 15% faster than Standard

Device Resources

Device Series	Logic Modules	Gates	User I/Os: CPGA 176-pin	CPGA 132-pin	CPGA 100-pin	PQFP 160-pin	PQFP 144-pin	PQFP 100-pin	PLCC 84-pin
A1280	1232	8000	140	–	–	124	–	–	–
A1240	684	4000	–	92	–	–	104	–	–
A1225	451	2500	–	–	83	–	–	–	67

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1,2,3]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Notes:

1. $V_{PP} = V_{CC}$, except during device programming.
2. $V_{SV} = V_{CC}$, except during device programming.
3. V_{KS} = GND, except during device programming.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range (Note 1)	0 to +70	-40 to +85	-55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) used for commercial and industrial; case temperature (T_C) used for military.

Electrical Specifications

Parameter		Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -10 mA)[2]	2.4						V
	(I_{OH} = -6 mA)	3.84						V
	(I_{OH} = -4 mA)			3.7		3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5					V
	(I_{OL} = 6 mA)		0.33		0.40		0.40	V
V_{IL}		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2,3]			10		10		10	pF
Standby Current, I_{CC}[4]			10		20		25	mA
Leakage Current[5]		-10	10	-10	10	-10	10	µA

Notes:

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 125°C}{20°C/W} = 1.2\ W$$

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
CPGA	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	2	20	8	°C/W
PQFP[1]	100	13	55	47	°C/W
	144	15	35	26	°C/W
	160	15	33	24	°C/W
PLCC	84	12	44	33	°C/W

Note:
1. Maximum Power Dissipation for PQFP Package = 2.0 Watts

Power Dissipation

$$P = [I_{CC} + I_{active}] \cdot V_{CC} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CC} - V_{OH}) \cdot M$$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing

I_{active} is the current flowing due to CMOS switching

I_{OL}, I_{OH} are TTL sink/source currents

V_{OL}, V_{OH} are TTL level output voltages

N equals the number of outputs driving TTL loads to V_{OL} and

M equal the number of outputs driving TTL loads to V_{OH}

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

10 mA x 5.25 V = 52.5 mW

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32 bit bus driving TTL loads will generate 42 mW ATT with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} \cdot V_{CC}^2 \cdot f \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF

V_{CC} is power supply in volts

f is the switching frequency in MHz

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

	C_{EQ} (pF)
Modules	7.7
Input Buffers	18.0
Output Buffers	25.0
Clock Buffer Loads	2.5

To calculate the active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power} = [(m \cdot 7.7 \cdot f_1) + (n \cdot 18.0 \cdot f_2) + (p \cdot (25.0 + C_L) \cdot f_3) + (q \cdot 2.5 \cdot f)] \cdot V_{CC}^2 \quad (2)$$

Where:

n = number of logic modules switching at frequency f_1

m = number of input buffers switching at frequency f_2

p = number of output buffers switching at frequency f_3

q = number of clock loads on the global clock network

f = frequency of global clock

f_1 = average logic module switching rate in MHz

f_2 = average input buffer switching rate in MHz

f_3 = average output buffer switching rate in MHz

C_L = output load capacitance

Determining Average Switching Frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

1/3 of I/O are Inputs

Average Input Frequency = F/5

2/3 of I/Os are Outputs

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

Estimated Power

The results of estimating active power are displayed in Figure 5. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

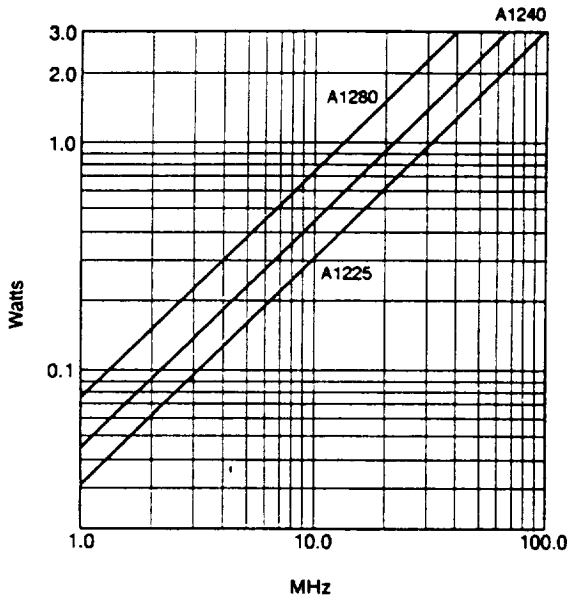
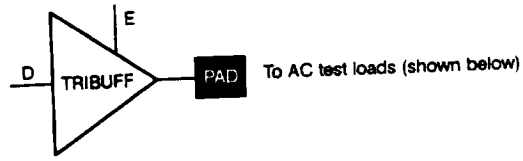
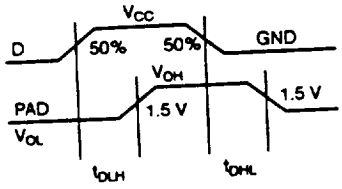


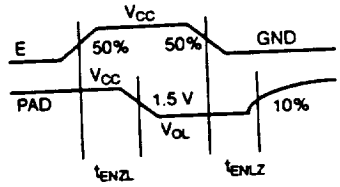
Figure 5. ACT 2 Power Estimates

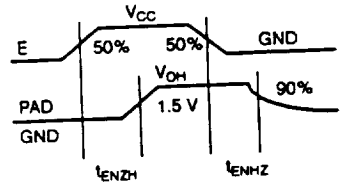
Parameter Measurement

Output Buffer Delays



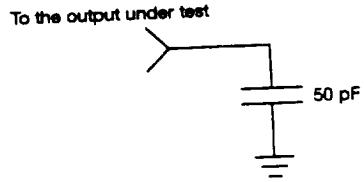




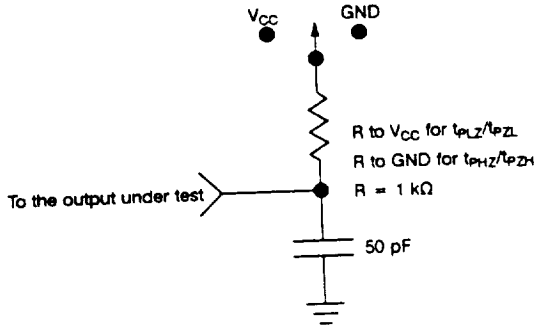


AC Test Loads

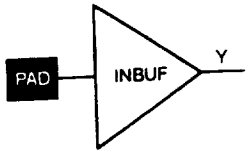
Load 1
(Used to measure propagation delay)

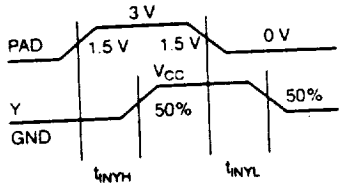


Load 2
(Used to measure rising/falling edges)

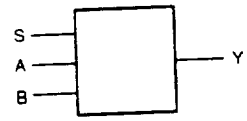


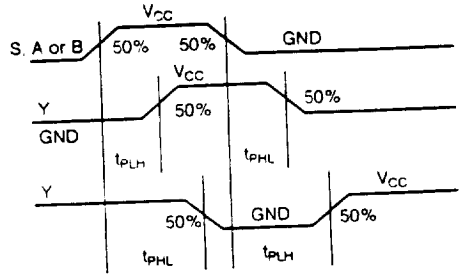
Input Buffer Delays





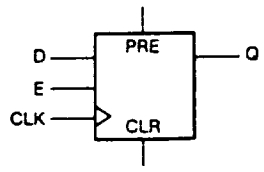
Combinatorial Macro Delays



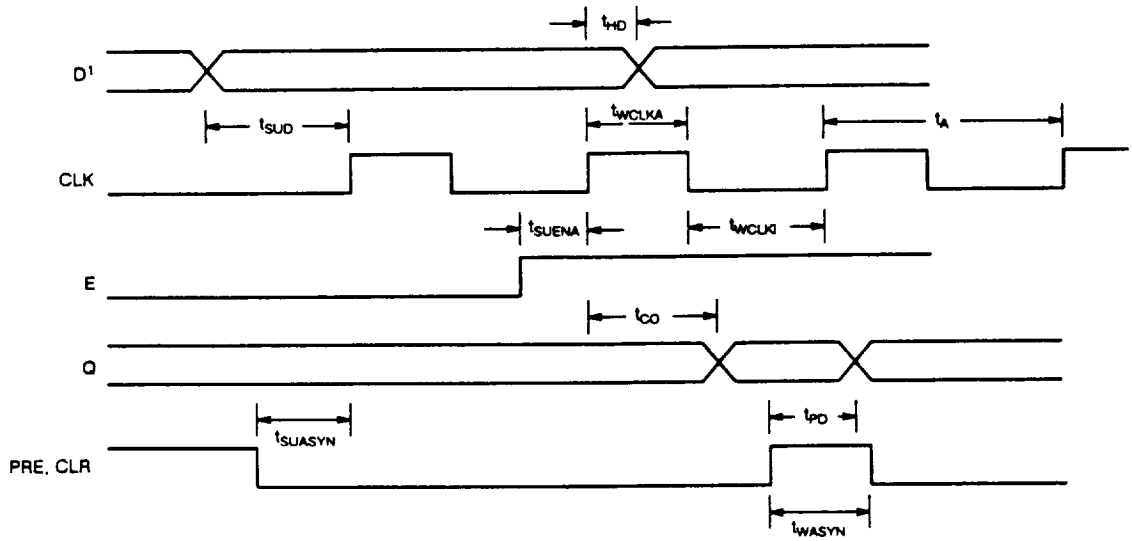


Sequential Timing Characteristics

Flip-Flops and Latches



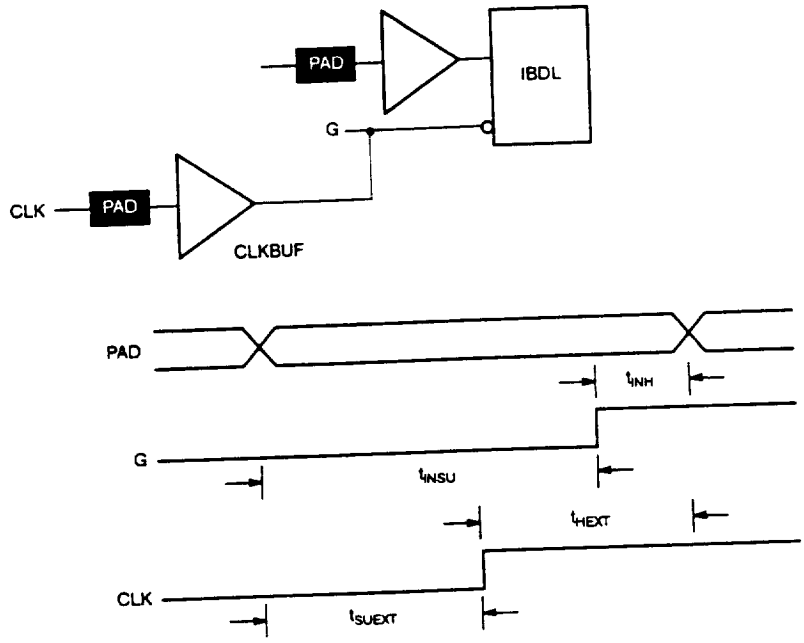
(Positive edge triggered)



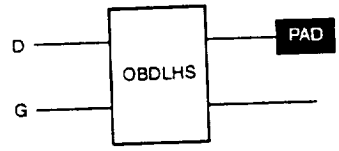
Notes:
1. D represents all data functions involving A, B, S for multiplexed flip-flops.

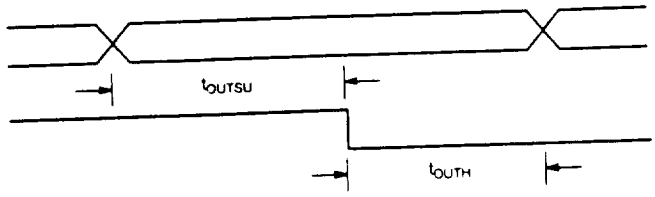
Sequential Timing Characteristics (continued)

Input Buffer Latches



Output Buffer Latches





Timing Characteristics

Timing characteristics for ACT arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all ACT 2 family members. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the users design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

The macro propagation delays shown in the Timing Characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on fully utilized devices (90% module utilization).

Critical Nets and Typical Nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to six percent of the nets in a design may be designated as *critical*, while ninety percent of the nets in a design are *typical*.

Fan-out Dependency

Propagation delays depend on the fan-out (number of loads) driven by a macro. Delay time increases when fan-out increases due to the capacitive loading of the macro's inputs, as well as the interconnect's resistance and capacitance.

Long Tracks

Some nets in the design use *long tracks*. Long tracks are special routing resources that span multiple rows or columns or modules, and are used frequently in large fan-out (> 10) situations. Long tracks employ three and sometimes four antifuse connections. This increased capacitance and resistance results in longer net delays for macros connected to long tracks. Typically up to six percent of the nets in a fully utilized device require long tracks. Long tracks contribute an additional 10 ns to 15 ns delay.

Timing Derating

Operating temperature, operating voltage and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for ACT 2 array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for ACT 2 applications. The derating curves in Figure 6 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curve is based on device junction temperature. Actual junction temperature is determined from Ambient Temperature, Power Dissipation, and Package Thermal characteristics.

Timing Derating Factor (x typical)

Commercial		Industrial		Military	
Best Case	**Worst Case**	**Best Case**	**Worst Case**	**Best Case**	**Worst Case**
0.40	1.40	0.37	1.50	0.35	1.6

Note:
Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

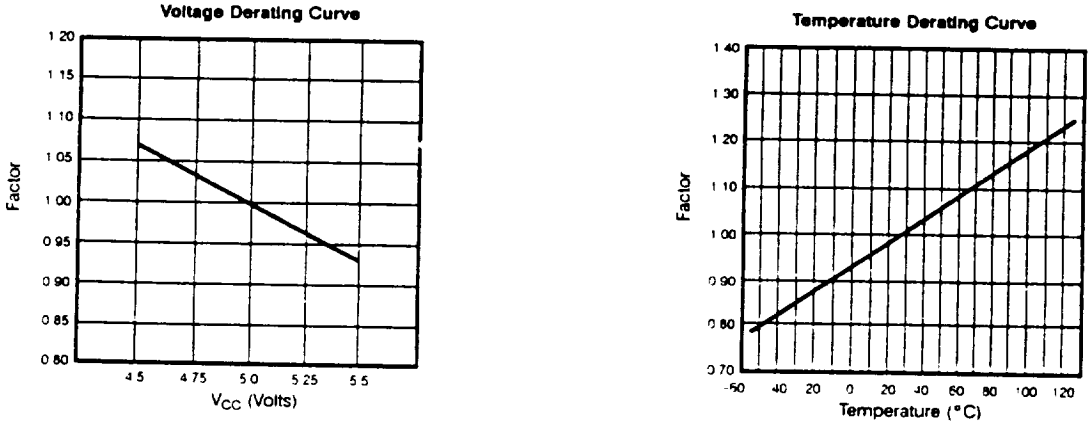


Figure 6. Derating Curves

A1280 Timing Characteristics

Propagation Delays (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD1}	Single Module	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD2}	Dual Module	Critical	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical	8.7	9.2	9.7	11.2	14.7	ns
t_{CO}	Sequential Clk to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{CO}	Sequential Clk to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{GO}	Latch G to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{GO}	Latch G to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD}	Asynchronous to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD}	Asynchronous to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns

Sequential Timing Characteristics (over Worst-Case Recommended Operating Conditions; No Further Derating Required)

Parameter	Description	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUD}	Flip-Flop Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{SUD}	Latch Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Latch Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop Data Input Hold		0.0		0.0		0.0	ns
t_{HD}	Latch Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop Enable Setup	5.0		6.0		7.5		ns
t_{WCLKA}	Flip-Flop Clock Active Pulse Width	7.5		8.25		9.0		ns
t_{WASYN}	Flip-Flop Asynchronous Pulse Width	7.5		8.25		9.0		ns
t_A	Flip-Flop Clock Input Period	18.0		20.0		22.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop Clock Frequency		48.0		43.0		39.0	MHz

Note:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs.

   Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280 Timing Characteristics (continued)

I/O Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.7	7.2	7.7	8.2	11.7	ns
t_{INYL}	Pad to Y Low	6.6	7.1	7.6	8.1	11.5	ns
t_{INGH}	G to Y High	6.6	7.2	7.7	8.2	11.7	ns
t_{INGL}	G to Y Low	6.4	6.9	7.5	8.0	11.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO = 384	Units
t_{CKH}	Input Low to High	9.1	10.1	12.3	ns
t_{CKL}	Input High to Low	9.1	10.2	12.5	ns
t_{PWH}	Minimum Pulse Width High	6.0	6.0	6.0	ns
t_{PWL}	Minimum Pulse Width Low	6.0	6.0	6.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold	7.0	8.0	11.2	ns
t_P	Minimum Period	15.0	18.0	20.0	ns
f_{MAX}	Maximum Frequency	66.0	55.0	50.0	MHz

Output Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1280-1 Timing Characteristics

Propagation Delays (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{PD1}	Single Module	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD1}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.9	8.3	8.7	10.0	13.0	ns
t_{PD2}	Sequential Clk to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{CO}	Latch G to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{GO}	Latch G to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{GO}	Asynchronous to Q	Critical	3.9	4.3	4.8	5.3	–	ns
t_{PD}	Asynchronous to Q	Typical	4.9	5.3	5.7	7.0	10.0	ns
t_{PD}								

Sequential Timing Characteristics (over Worst-Case Recommended Operating Conditions; No Further Derating Required)

Parameter	Description	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUD}	Flip-Flop Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{SUD}	Latch Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Latch Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop Data Input Hold		0.0		0.0		0.0	ns
t_{HD}	Latch Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop Enable Setup	5.0		6.0		7.5		ns
t_{WCLKA}	Flip-Flop Clock Active Pulse Width	6.5		7.8		9.0		ns
t_{WASYN}	Flip-Flop Asynchronous Pulse Width	6.5		7.8		9.0		ns
t_A	Flip-Flop Clock Input Period	15.0		18.0		20.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop Clock Frequency		55.0		50.0		45.0	MHz

Note:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs.

   Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280-1 Timing Characteristics (continued)

I/O Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INYL}	Pad to Y Low	5.9	6.4	6.8	7.3	10.4	ns
t_{INGH}	G to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INGL}	G to Y Low	5.9	6.4	6.8	7.3	10.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO = 384	Units
t_{CKH}	Input Low to High	7.8	8.7	10.4	ns
t_{CKL}	Input High to Low	7.8	8.8	10.6	ns
t_{PWH}	Minimum Pulse Width High	5.1	5.5	6.0	ns
t_{PWL}	Minimum Pulse Width Low	5.1	5.5	6.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold	7.0	8.0	11.2	ns
t_P	Minimum Period	12.0	15.0	16.6	ns
f_{MAX}	Maximum Frequency	80.0	66.0	60.0	MHz

Output Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

SECTION 3.4
Calculation of Current Density

JET PROPULSION LABORATORY
M. Sandor

VENDOR: ACTEL

CONSTANT CURRENT DENSITY CALCULATION FOR SINGLE OR MULTIPLE VIA FROM METAL 1 TO SILICON

Technology:CMOS 1.2um; Metal 1 is AL-Si(1%)-Cu(0.5%); LOCOS
Passivation is 300nm SiO2,800 nm SiN

	Enter	Unit	Calculation		
Metal 1width	3.20	um			
Metal 1 thickness	0.80	um	A1 in cm2 =	3.4558E-09	
			CD@A1 =	2.89E+05	
Via opening size (oxide)	1.3	um			
Via size at A1(Silicon)	1.20	um	A1 in um2 =	0.345576	
Metal 1 thickness at step	0.10	um			
Step coverage at via			12.5%		
Worst case current in via(derated) (out buffers are rated at 4.0ma)	1.00	ma			
Temperature(max operationg + Junct rise)	150	Cent			
VDD	5.00	Volts			

Case 1:Current density in single via [This is worst case]	=		2.89E+05	A/cm2
			2.89	ma/um2
Case 2: C.D. with multiple via [This is typical case]	=	2 cts.	1.45E+05	A/cm2
Case 3: C.D. w/o via(interconnect) [This is best case]	=		3.91E+04	A/cm2

t50 and t.01 TIME TO FAILURE (for log-normal distribution)
where t.50 = A.50 * J^-n * exp(Ea/KT) [BLACK'S EQUATION]

	Enter	Unit	Calculation	Unit
A50(constant) =	5.00E+07	hrs	A.01(constant) 1.39E+07	hrs
n(current density exponent) =	2		where A.01 = A50 * e(sigma * Z)	
k(Boltzmann constant) =	8.62E-05	ev/K	sigma of failure distribution = ln(t.50/t.16)/1	
T(temperature) =	423	K	Z = from statistics table	
Ea(activation energy for EM) = [for Al-Si-Cu]	0.63	ev		

Current density in single via [This is worst case]	=	2.89E+05	A/cm2	t50 =	19133 hrs 2.2 yrs
				t.01 =	5312 hrs 0.6 yrs
Reduced C.D. with multiple via [This is typical case]	=	1.45E+05	A/cm2	t50 =	76531 hrs 8.7 yrs
				t.01 =	21246 hrs 2.4 yrs
Current density interconnect [This is best case]	=	3.91E+04	A/cm2	t50 =	1049947 hrs 119.9 yrs
				t.01 =	291487 hrs 33.3 yrs

Case 1[Duty cycle = .50]
t50(pulse) = 8.7 yrs
t.01(pulse) = 2.4 yrs

Figure 4

JET PROPULSION LABORATORY
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METAL 1 TIME TO FAILURE (t.01) FOR ELECTROMIGRATION

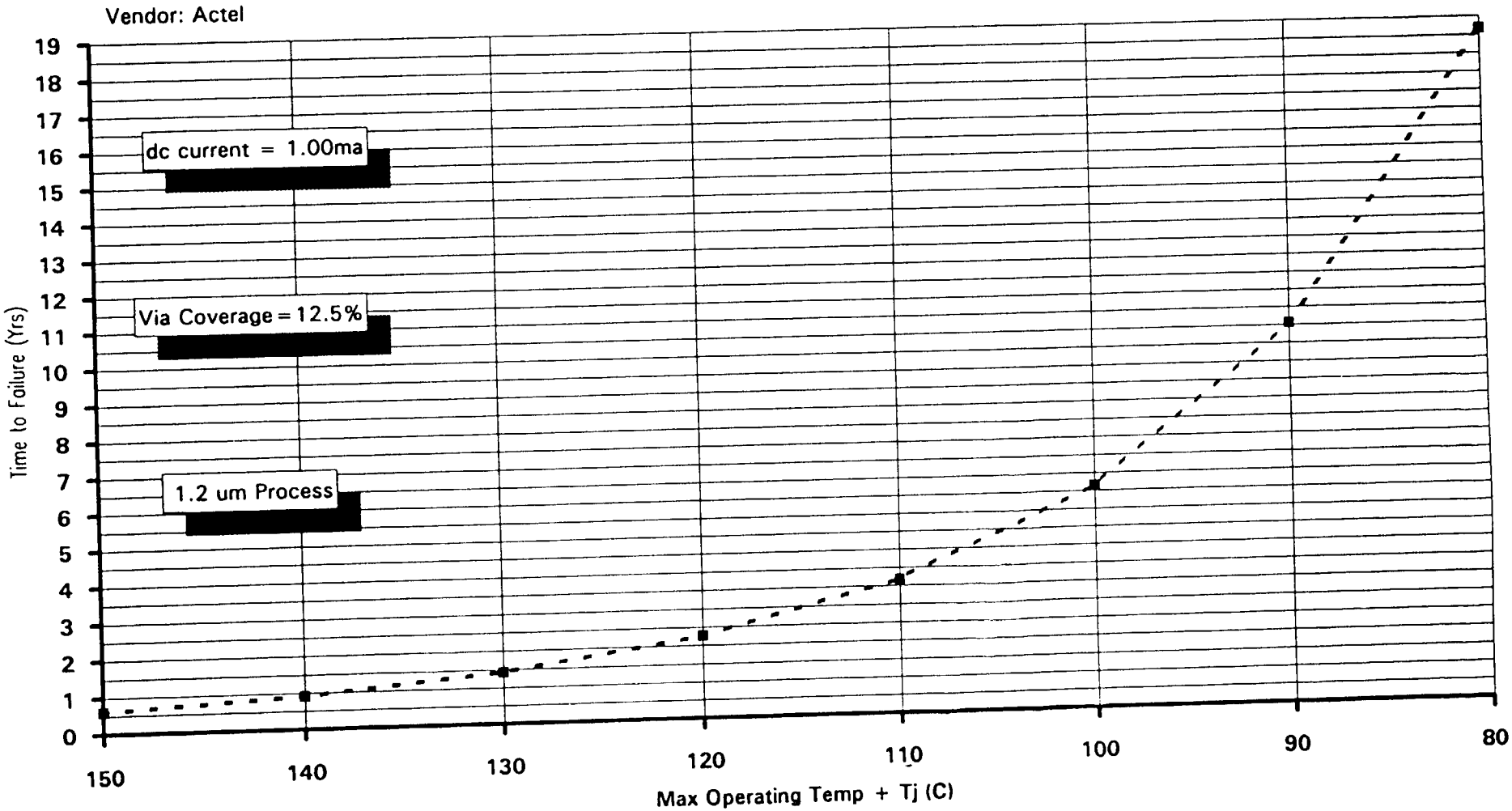

Figure 8

JET PROPULSION LABORATORY
M. Sandor

VENDOR: ACTEL

CONSTANT CURRENT DENSITY CALCULATION FOR SINGLE OR MULTIPLE VIA FROM METAL 1 TO SILICON

Technology: CMOS 1.2um; MetaL 1 is AL-Si(1%)-Cu(0.5%); LOCOS
Passivation is 300nm SiO2, 800 nm SiN

	Enter	Unit	Calculation	
Metal 1 width	3.20	um		
Metal 1 thickness	0.80	um	A1 in cm2 =	3.4558E-09
			CD@A1 =	1.16E+06
Via opening size (oxide)	1.3	um		
Via size at A1 (Silicon)	1.20	um	A1 in um2 =	0.345576
Metal 1 thickness at step	0.10	um		
Step coverage at via			12.5%	
Worst case current in via(derated) (output buffers are rated at 4.0ma)	4.00	ma		
Temperature(max operationg + Junct rise)	150	Cent		
VDD	5.00	Volts		

t50 and t.01 TIME TO FAILURE (for log-normal distribution)
where t.50 = A.50 * J^-n * exp(Ea/KT) [BLACK'S EQUATION]

	Enter	Unit	Calculation	Unit
A50(constant) =	5.00E+07	hrs	A.01(constant) 1.39E+07	hrs
			where A.01 = A50 * e(sigma * Z)	
n(current density exponent) =	2		sigma of failure distribution = ln(t.50/t.16)/1	
			Z = from statistics table	
k(Boltzmann constant) =	8.62E-05	ev/K		
T(temperature) =	423	K		
Ea(activation energy for EM) = [for Al-Si-Cu]	0.63	ev		

Case 1: Current density in single via = [This is worst case]			1.16E+06	A/cm2	Current density in single via = [This is worst case]	1.16E+06 A/cm2	t50 = 1196 hrs 0.1 yrs t.01 = 332 hrs 0.0 yrs
			11.57	ma/um2			
Case 2: C.D. with multiple via = [This is typical case]	2	cts.	5.79E+05	A/cm2	Reduced C.D. with multiple via = [This is typical case]	5.79E+05 A/cm2	t50 = 4783 hrs 0.5 yrs t.01 = 1328 hrs 0.2 yrs
Case 3: C.D. w/o via(interconnect) = [This is best case]			1.56E+05	A/cm2	Current density interconnect = [This is best case]	1.56E+05 A/cm2	t50 = 65622 hrs 7.5 yrs t.01 = 18218 hrs 2.1 yrs

Case 1 [Duty cycle = .50]
t50(pulse) = 0.5 yrs
t.01(pulse) = 0.2 yrs

Figure 4

JET PROPULSION LABORATORY
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METAL 1 TIME TO FAILURE (t.01) FOR ELECTROMIGRATION

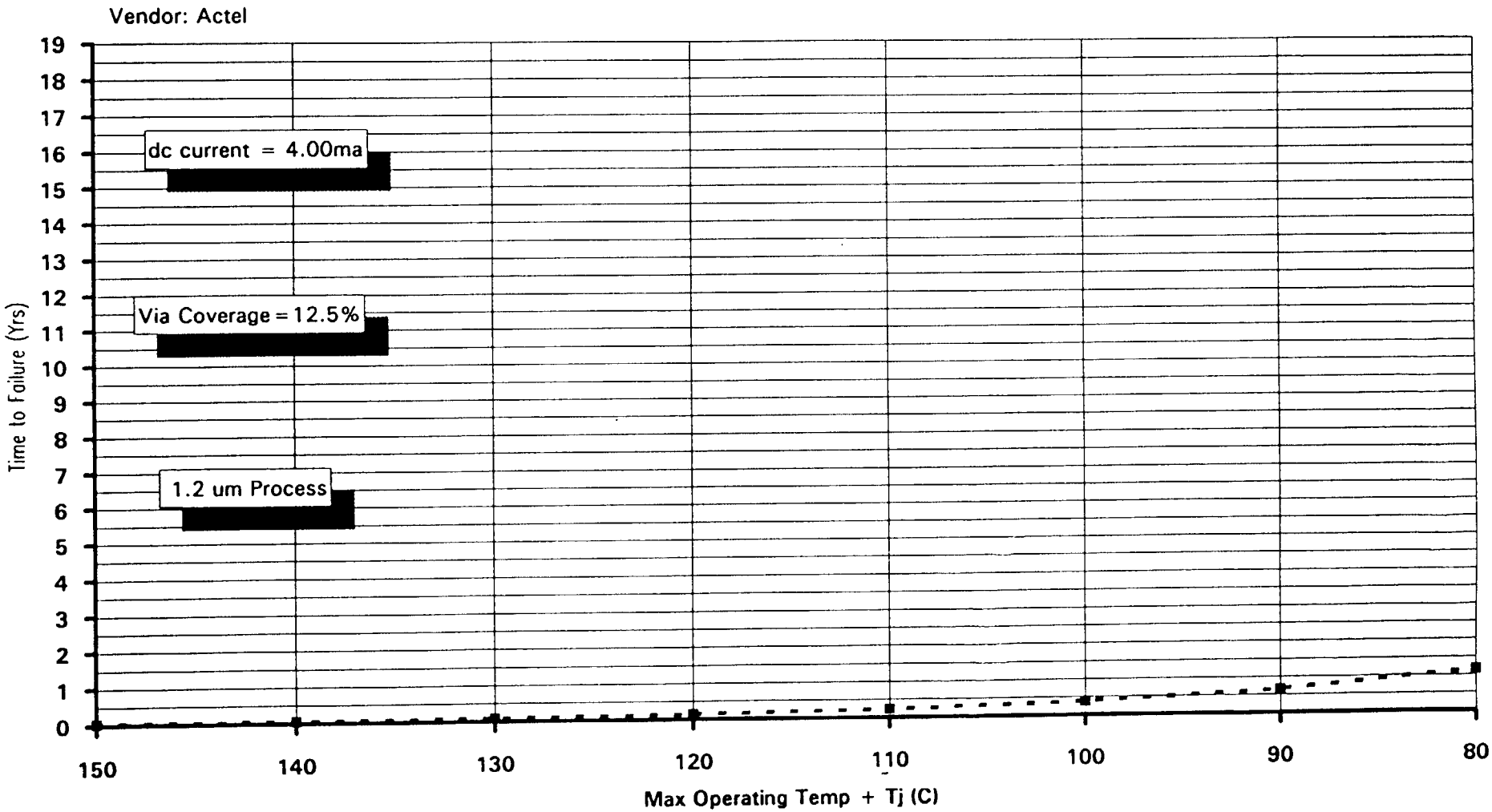

Figure 8

SECTION 3.5
Electrical Characterization Data

Example

JPL Beta-12 A128C FPGA Temp: 25 Ser #: 3
22-JUN-1992 12:12:23.82 Datecode: 9143 Page: 1
Source file: Beta12.C:H44
Post 500 hrs

Functional test params: Vcc = 4.50V, Vih = 3.00V, Vil = 0	C.00V	Tc =	0 to 1299	1000.0nS.	pass	ft4.5
Functional test params: Vcc = 4.75V, Vih = 3.00V, Vil = 0	C.00V	Tc =	0 to 1299	1000.0nS.	pass	ft4.7
Functional test params: Vcc = 5.00V, Vih = 3.00V, Vil = 0	C.00V	Tc =	0 to 1299	1000.0nS.	pass	ft5.0
Functional test params: Vcc = 5.25V, Vih = 3.00V, Vil = 0	C.00V	Tc =	0 to 1299	1000.0nS.	pass	ft5.2
Functional test params: Vcc = 5.50V, Vih = 3.00V, Vil = 0	C.00V	Tc =	0 to 1299	1000.0nS.	pass	ft5.5

VOH params: Vcc = 4.50V, Vih = 3.000V, Vil = 0.000V, Io = -4.000mA.
Limits: 3.700 V minimum, 5.500 V maximum.

Q0	4.210 V	Q1	4.205 V	Q2	4.205 V
Q3	4.188 V	Q0B	4.205 V	Q1B	4.210 V
Q2B	4.203 V	Q3B	4.190 V	TOUTA	4.210 V
QOUTA	4.205 V	TOUTB	4.207 V	QOUTB	4.207 V
MKTOUT	4.205 V	MKOUTB	4.205 V	MMOUT	4.198 V
COUT	4.198 V	P0	4.193 V	P1	4.203 V
P2	4.190 V	P3	4.193 V	P4	4.200 V
P5	4.203 V	P6	4.200 V	P7	4.200 V
DEC0	4.188 V	DEC1	4.203 V	DEC2	4.193 V
DEC3	4.200 V	DEC4	4.190 V	DEC5	4.200 V
DEC6	4.203 V	DEC7	4.188 V	DEC8	4.188 V
DEC9	4.193 V	DEC10	4.198 V	DEC11	4.212 V
DEC12	4.203 V	DEC13	4.161 V	DEC14	4.210 V
DEC15	4.200 V	DEC16	4.198 V	DEC17	4.198 V
DEC18	4.205 V	DEC19	4.198 V	DEC20	4.193 V
DEC21	4.198 V	DEC22	4.198 V	DEC23	4.195 V
DEC24	4.190 V	DEC25	4.190 V	DEC26	4.195 V
DEC27	4.195 V	DEC28	4.190 V	DEC29	4.198 V
DEC30	4.205 V	DEC31	4.183 V	DEC32	4.203 V
DEC33	4.207 V	DEC34	4.200 V	DEC35	4.195 V
DEC36	4.203 V	DEC37	4.212 V	DEC38	4.205 V
DEC39	4.193 V	MOUT40	4.198 V	MOUT41	4.212 V
MOUT42	4.203 V	MOUT43	4.205 V	MOUT44	4.198 V
MOUT45	4.200 V	MOUT46	4.198 V	MOUT47	4.203 V
DEC0B	4.188 V	DEC1B	4.193 V	DEC2B	4.198 V
DEC3B	4.203 V	DEC4B	4.203 V	DEC5B	4.181 V
DEC6B	4.183 V	DEC7B	4.200 V	DEC8B	4.203 V
DEC9B	4.190 V	DEC10B	4.207 V	DEC11B	4.210 V
DEC12B	4.195 V	DEC13B	4.200 V	DEC14B	4.205 V
DEC15B	4.203 V	DEC16B	4.203 V	DEC17B	4.200 V
DEC18B	4.203 V	DEC19B	4.205 V	DEC20B	4.203 V
DEC21B	4.200 V	DEC22B	4.181 V	DEC23B	4.207 V
DEC24B	4.190 V	DEC25B	4.205 V	DEC26B	4.210 V
DEC27B	4.186 V	DEC28B	4.183 V	DEC29B	4.195 V
DEC30B	4.188 V	DEC31B	4.188 V	DEC32B	4.205 V
DEC33B	4.185 V	DEC34B	4.205 V	DEC35B	4.207 V
DEC36B	4.210 V	DEC37B	4.215 V	DEC38B	4.205 V
DEC39B	4.205 V	OUT40B	4.205 V	OUT41B	4.205 V
OUT42B	4.205 V	OUT43B	4.207 V	OUT44B	4.200 V
OUT45B	4.205 V	OUT46B	4.205 V	OUT47B	4.207 V

VOH params: Vcc = 4.75V, Vih = 3.000V, Vil = 0.000V, Io = -4.000mA.
Limits: 3.700 V minimum, 5.500 V maximum.

Q0	4.469 V	Q1	4.464 V	Q2	4.467 V
Q3	4.447 V	Q0B	4.467 V	Q1B	4.472 V
Q2B	4.467 V	Q3B	4.450 V	TOUTA	4.469 V
QOUTA	4.467 V	TOUTB	4.469 V	QOUTB	4.467 V
MKTOUT	4.469 V	MKOUTB	4.464 V	MMOUT	4.459 V
COUT	4.459 V	P0	4.455 V	P1	4.464 V
P2	4.452 V	P3	4.455 V	P4	4.462 V
P5	4.467 V	P6	4.462 V	P7	4.462 V
DEC0	4.450 V	DEC1	4.464 V	DEC2	4.455 V

DEC3	4.462 V	DEC4	4.450 V	DEC5	4.462 V
DEC6	4.464 V	DEC7	4.450 V	DEC8	4.452 V
DEC9	4.452 V	DEC10	4.459 V	DEC11	4.472 V
DEC12	4.467 V	DEC13	4.420 V	DEC14	4.469 V
DEC15	4.462 V	DEC16	4.462 V	DEC17	4.459 V
DEC18	4.464 V	DEC19	4.459 V	DEC20	4.457 V
DEC21	4.459 V	DEC22	4.459 V	DEC23	4.455 V
DEC24	4.450 V	DEC25	4.452 V	DEC26	4.459 V
DEC27	4.457 V	DEC28	4.450 V	DEC29	4.457 V
DEC30	4.469 V	DEC31	4.442 V	DEC32	4.464 V
DEC33	4.469 V	DEC34	4.462 V	DEC35	4.455 V
DEC36	4.464 V	DEC37	4.472 V	DEC38	4.467 V
DEC39	4.455 V	MOUT40	4.459 V	MOUT41	4.472 V
MOUT42	4.464 V	MOUT43	4.464 V	MOUT44	4.459 V
MOUT45	4.462 V	MOUT46	4.462 V	MOUT47	4.464 V
DEC0B	4.450 V	DEC1B	4.452 V	DEC2B	4.459 V
DEC3B	4.464 V	DEC4B	4.464 V	DEC5B	4.442 V
DEC6B	4.445 V	DEC7B	4.462 V	DEC8B	4.464 V
DEC9B	4.450 V	DEC10B	4.467 V	DEC11B	4.472 V
DEC12B	4.457 V	DEC13B	4.462 V	DEC14B	4.464 V
DEC15B	4.464 V	DEC16B	4.464 V	DEC17B	4.462 V
DEC18B	4.464 V	DEC19B	4.467 V	DEC20B	4.464 V
DEC21B	4.462 V	DEC22B	4.445 V	DEC23B	4.467 V
DEC24B	4.450 V	DEC25B	4.467 V	DEC26B	4.469 V
DEC27B	4.447 V	DEC28B	4.445 V	DEC29B	4.455 V
DEC30B	4.450 V	DEC31B	4.447 V	DEC32B	4.467 V
DEC33B	4.447 V	DEC34B	4.464 V	DEC35B	4.467 V
DEC36B	4.469 V	DEC37B	4.477 V	DEC38B	4.467 V
DEC39B	4.467 V	OUT40B	4.467 V	OUT41B	4.464 V
OUT42B	4.467 V	OUT43B	4.469 V	OUT44B	4.459 V
OUT45B	4.467 V	OUT46B	4.469 V	OUT47B	4.469 V

VOH params: Vcc = 5.00V, Vih = 3.000V, Vil = 0.000V, Io = -4.000mA.
Limits: 3.700 V minimum, 5.500 V maximum.

C0	4.731 V	C1	4.726 V	C2	4.726 V
C3	4.704 V	C0B	4.720 V	C1B	4.731 V
C2B	4.726 V	C3B	4.709 V	TOUTA	4.731 V
COUTA	4.728 V	TOUTB	4.726 V	COUTB	4.726 V
MKTOUT	4.720 V	MKOUTB	4.720 V	MMOUT	4.721 V
COUT	4.719 V	P0	4.714 V	P1	4.724 V
P2	4.714 V	P3	4.714 V	P4	4.724 V
P5	4.720 V	P6	4.721 V	P7	4.721 V
DEC0	4.711 V	DEC1	4.724 V	DEC2	4.714 V
DEC3	4.721 V	DEC4	4.709 V	DEC5	4.721 V
DEC6	4.724 V	DEC7	4.709 V	DEC8	4.711 V
DEC9	4.711 V	DEC10	4.721 V	DEC11	4.733 V
DEC12	4.726 V	DEC13	4.677 V	DEC14	4.731 V
DEC15	4.721 V	DEC16	4.721 V	DEC17	4.721 V
DEC18	4.726 V	DEC19	4.719 V	DEC20	4.716 V
DEC21	4.719 V	DEC22	4.721 V	DEC23	4.716 V
DEC24	4.709 V	DEC25	4.709 V	DEC26	4.719 V
DEC27	4.716 V	DEC28	4.711 V	DEC29	4.719 V
DEC30	4.728 V	DEC31	4.704 V	DEC32	4.724 V
DEC33	4.728 V	DEC34	4.721 V	DEC35	4.719 V
DEC36	4.724 V	DEC37	4.731 V	DEC38	4.726 V
DEC39	4.716 V	MOUT40	4.721 V	MOUT41	4.736 V
MOUT42	4.726 V	MOUT43	4.724 V	MOUT44	4.719 V
MOUT45	4.724 V	MOUT46	4.721 V	MOUT47	4.726 V
DEC0B	4.709 V	DEC1B	4.711 V	DEC2B	4.719 V

DEC3B	4.726 V	DEC4B	4.726 V	DEC5B	4.702 V
DEC6B	4.704 V	DEC7B	4.724 V	DEC8B	4.721 V
DEC9B	4.711 V	DEC10B	4.728 V	DEC11B	4.731 V
DEC12B	4.716 V	DEC13B	4.724 V	DEC14B	4.726 V
DEC15B	4.724 V	DEC16B	4.724 V	DEC17B	4.721 V
DEC18B	4.724 V	DEC19B	4.726 V	DEC20B	4.726 V
DEC21B	4.724 V	DEC22B	4.704 V	DEC23B	4.728 V
DEC24B	4.709 V	DEC25B	4.726 V	DEC26B	4.731 V
DEC27B	4.706 V	DEC28B	4.704 V	DEC29B	4.714 V
DEC30B	4.709 V	DEC31B	4.706 V	DEC32B	4.728 V
DEC33B	4.709 V	DEC34B	4.726 V	DEC35B	4.726 V
DEC36B	4.728 V	DEC37B	4.736 V	DEC38B	4.728 V
DEC39B	4.726 V	OUT40B	4.726 V	OUT41B	4.726 V
OUT42B	4.726 V	OUT43B	4.728 V	OUT44B	4.721 V
OUT45B	4.726 V	OUT46B	4.726 V	OUT47B	4.731 V

VOH params: Vcc = 5.25V, Vih = 3.000V, Vil = 0.000V, Io = -4.000mA.
Limits: 3.700 V minimum, 5.500 V maximum.

Q0	4.986 V	Q1	4.985 V	Q2	4.985 V
Q3	4.961 V	Q0B	4.985 V	Q1B	4.990 V
Q2B	4.985 V	Q3B	4.968 V	TOUTA	4.990 V
QOUTA	4.985 V	TOUTB	4.985 V	COUTB	4.985 V
MKTOUT	4.988 V	MKOUTB	4.985 V	MMOUT	4.978 V
COUT	4.978 V	P0	4.973 V	P1	4.980 V
P2	4.971 V	P3	4.976 V	P4	4.980 V
P5	4.985 V	P6	4.980 V	P7	4.980 V
DEC0	4.966 V	DEC1	4.983 V	DEC2	4.973 V
DEC3	4.980 V	DEC4	4.966 V	DEC5	4.980 V
DEC6	4.983 V	DEC7	4.966 V	DEC8	4.968 V
DEC9	4.971 V	DEC10	4.978 V	DEC11	4.990 V
DEC12	4.985 V	DEC13	4.934 V	DEC14	4.988 V
DEC15	4.985 V	DEC16	4.980 V	DEC17	4.980 V
DEC18	4.985 V	DEC19	4.978 V	DEC20	4.976 V
DEC21	4.978 V	DEC22	4.980 V	DEC23	4.976 V
DEC24	4.968 V	DEC25	4.968 V	DEC26	4.976 V
DEC27	4.973 V	DEC28	4.966 V	DEC29	4.976 V
DEC30	4.986 V	DEC31	4.961 V	DEC32	4.983 V
DEC33	4.986 V	DEC34	4.980 V	DEC35	4.976 V
DEC36	4.985 V	DEC37	4.990 V	DEC38	4.988 V
DEC39	4.973 V	MOUT40	4.980 V	MOUT41	4.993 V
MOUT42	4.983 V	MOUT43	4.985 V	MOUT44	4.980 V
MOUT45	4.983 V	MOUT46	4.980 V	MOUT47	4.983 V
DEC0B	4.966 V	DEC1B	4.971 V	DEC2B	4.978 V
DEC3B	4.985 V	DEC4B	4.985 V	DEC5B	4.961 V
DEC6B	4.963 V	DEC7B	4.980 V	DEC8B	4.983 V
DEC9B	4.968 V	DEC10B	4.988 V	DEC11B	4.990 V
DEC12B	4.973 V	DEC13B	4.980 V	DEC14B	4.985 V
DEC15B	4.983 V	DEC16B	4.983 V	DEC17B	4.980 V
DEC18B	4.983 V	DEC19B	4.985 V	DEC20B	4.985 V
DEC21B	4.980 V	DEC22B	4.963 V	DEC23B	4.988 V
DEC24B	4.966 V	DEC25B	4.985 V	DEC26B	4.988 V
DEC27B	4.963 V	DEC28B	4.961 V	DEC29B	4.971 V
DEC30B	4.966 V	DEC31B	4.966 V	DEC32B	4.985 V
DEC33B	4.966 V	DEC34B	4.985 V	DEC35B	4.985 V
DEC36B	4.986 V	DEC37B	4.993 V	DEC38B	4.988 V
DEC39B	4.985 V	OUT40B	4.988 V	OUT41B	4.985 V
OUT42B	4.985 V	OUT43B	4.988 V	OUT44B	4.980 V
OUT45B	4.985 V	OUT46B	4.985 V	OUT47B	4.988 V

VOH params: Vcc = 5.50V, Vih = 3.000V, Vil = 0.000V, Io = -4.000mA.
Limits: 3.700 V minimum, 5.500 V maximum.

Q0	5.247 V	Q1	5.242 V	Q2	5.242 V
Q3	5.218 V	Q0B	5.245 V	Q1B	5.247 V
Q2B	5.242 V	Q3B	5.223 V	TOUTA	5.247 V
QOUTA	5.245 V	TOUTB	5.247 V	QOUTB	5.247 V
MKTOUT	5.245 V	MKOUTB	5.245 V	MMOUT	5.237 V
COUT	5.237 V	P0	5.232 V	P1	5.240 V
P2	5.230 V	P3	5.232 V	P4	5.240 V
P5	5.242 V	P6	5.237 V	P7	5.240 V
DEC0	5.223 V	DEC1	5.240 V	DEC2	5.230 V
DEC3	5.235 V	DEC4	5.223 V	DEC5	5.240 V
DEC6	5.242 V	DEC7	5.223 V	DEC8	5.227 V
DEC9	5.227 V	DEC10	5.237 V	DEC11	5.250 V
DEC12	5.245 V	DEC13	5.188 V	DEC14	5.247 V
DEC15	5.240 V	DEC16	5.237 V	DEC17	5.237 V
DEC18	5.242 V	DEC19	5.237 V	DEC20	5.235 V
DEC21	5.237 V	DEC22	5.235 V	DEC23	5.235 V
DEC24	5.225 V	DEC25	5.225 V	DEC26	5.232 V
DEC27	5.232 V	DEC28	5.225 V	DEC29	5.232 V
DEC30	5.245 V	DEC31	5.220 V	DEC32	5.240 V
DEC33	5.245 V	DEC34	5.240 V	DEC35	5.232 V
DEC36	5.242 V	DEC37	5.250 V	DEC38	5.245 V
DEC39	5.232 V	MOUT40	5.237 V	MOUT41	5.250 V
MOUT42	5.242 V	MOUT43	5.240 V	MOUT44	5.237 V
MOUT45	5.240 V	MOUT46	5.240 V	MOUT47	5.240 V
DEC0B	5.223 V	DEC1B	5.227 V	DEC2B	5.232 V
DEC3B	5.242 V	DEC4B	5.245 V	DEC5B	5.215 V
DEC6B	5.218 V	DEC7B	5.240 V	DEC8B	5.240 V
DEC9B	5.225 V	DEC10B	5.247 V	DEC11B	5.250 V
DEC12B	5.232 V	DEC13B	5.240 V	DEC14B	5.245 V
DEC15B	5.242 V	DEC16B	5.242 V	DEC17B	5.240 V
DEC18B	5.240 V	DEC19B	5.245 V	DEC20B	5.242 V
DEC21B	5.240 V	DEC22B	5.223 V	DEC23B	5.245 V
DEC24B	5.223 V	DEC25B	5.245 V	DEC26B	5.247 V
DEC27B	5.223 V	DEC28B	5.218 V	DEC29B	5.230 V
DEC30B	5.223 V	DEC31B	5.220 V	DEC32B	5.245 V
DEC33B	5.225 V	DEC34B	5.242 V	DEC35B	5.242 V
DEC36B	5.245 V	DEC37B	5.252 V	DEC38B	5.242 V
DEC39B	5.245 V	OUT40B	5.245 V	OUT41B	5.237 V
OUT42B	5.245 V	OUT43B	5.247 V	OUT44B	5.245 V
OUT45B	5.242 V	OUT46B	5.245 V	OUT47B	

JPL Beta-12 A128C FPGA
22-JUN-1992 12:12:46.67 Datecode: 9143 Temp: 25 Ser #: 3
Source file: Beta12.C:H44 Page: 3
Post 500 hrs

VOL params: Vcc = 4.50V, Vih = 3.000V, Vil = 0.000V, Io = 6.000mA.
Limits: 0.000 V minimum, 400.0mV maximum.

Q0	137.0mV	Q1	134.5mV	Q2	134.5mV
Q3	137.0mV	Q0B	137.0mV	Q1B	139.4mV
Q2B	137.0mV	Q3B	139.4mV	TOUTA	141.9mV
QOUTA	141.9mV	TOUTB	139.4mV	QOUTB	139.4mV
MKTOUT	139.4mV	MKOUTB	139.4mV	MMOUT	139.4mV
COUT	139.4mV	P0	134.5mV	P1	137.0mV
P2	134.5mV	P3	149.2mV	P4	134.5mV
P5	137.0mV	P6	137.0mV	P7	134.5mV
DEC0	137.0mV	DEC1	139.4mV	DEC2	137.0mV
DEC3	134.5mV	DEC4	139.4mV	DEC5	141.9mV
DEC6	137.0mV	DEC7	139.4mV	DEC8	159.0mV
DEC9	134.5mV	DEC10	134.5mV	DEC11	137.0mV
DEC12	137.0mV	DEC13	159.0mV	DEC14	141.9mV
DEC15	139.4mV	DEC16	134.5mV	DEC17	134.5mV
DEC18	137.0mV	DEC19	134.5mV	DEC20	137.0mV
DEC21	134.5mV	DEC22	134.5mV	DEC23	137.0mV
DEC24	132.1mV	DEC25	137.0mV	DEC26	134.5mV
DEC27	134.5mV	DEC28	134.5mV	DEC29	132.1mV
DEC30	141.9mV	DEC31	134.5mV	DEC32	137.0mV
DEC33	139.4mV	DEC34	134.5mV	DEC35	139.4mV
DEC36	139.4mV	DEC37	139.4mV	DEC38	137.0mV
DEC39	141.9mV	MOUT40	137.0mV	MOUT41	139.4mV
MOUT42	139.4mV	MOUT43	141.9mV	MOUT44	137.0mV
MOUT45	134.5mV	MOUT46	137.0mV	MOUT47	141.9mV
DEC0B	134.5mV	DEC1B	134.5mV	DEC2B	134.5mV
DEC3B	139.4mV	DEC4B	139.4mV	DEC5B	134.5mV
DEC6B	134.5mV	DEC7B	137.0mV	DEC8B	137.0mV
DEC9B	137.0mV	DEC10B	137.0mV	DEC11B	139.4mV
DEC12B	139.4mV	DEC13B	139.4mV	DEC14B	139.4mV
DEC15B	137.0mV	DEC16B	139.4mV	DEC17B	134.5mV
DEC18B	137.0mV	DEC19B	137.0mV	DEC20B	137.0mV
DEC21B	134.5mV	DEC22B	154.1mV	DEC23B	139.4mV
DEC24B	134.5mV	DEC25B	137.0mV	DEC26B	137.0mV
DEC27B	134.5mV	DEC28B	137.0mV	DEC29B	134.5mV
DEC30B	134.5mV	DEC31B	134.5mV	DEC32B	137.0mV
DEC33B	137.0mV	DEC34B	137.0mV	DEC35B	141.9mV
DEC36B	139.4mV	DEC37B	141.9mV	DEC38B	141.9mV
DEC39B	134.5mV	OUT40B	137.0mV	OUT41B	134.5mV
OUT42B	144.3mV	OUT43B	137.0mV	OUT44B	139.4mV
OUT45B	137.0mV	OUT46B	139.4mV	OUT47B	137.0mV

VOL params: Vcc = 4.75V, Vih = 3.000V, Vil = 0.000V, Io = 6.000mA.
Limits: 0.000 V minimum, 400.0mV maximum.

Q0	132.1mV	Q1	132.1mV	Q2	132.1mV
Q3	134.5mV	Q0B	134.5mV	Q1B	134.5mV
Q2B	132.1mV	Q3B	137.0mV	TOUTA	134.5mV
QOUTA	137.0mV	TOUTB	134.5mV	QOUTB	134.5mV
MKTOUT	134.5mV	MKOUTB	134.5mV	MMOUT	134.5mV
COUT	137.0mV	P0	129.6mV	P1	132.1mV
P2	132.1mV	P3	144.3mV	P4	129.6mV
P5	132.1mV	P6	134.5mV	P7	129.6mV
DEC0	132.1mV	DEC1	137.0mV	DEC2	132.1mV

DEC3	132.1mV	DEC4	134.5mV	DEC5	137.0mV
DEC6	132.1mV	DEC7	134.5mV	DEC8	154.1mV
DEC9	129.6mV	DEC10	129.6mV	DEC11	129.6mV
DEC12	132.1mV	DEC13	154.1mV	DEC14	137.0mV
DEC15	139.4mV	DEC16	132.1mV	DEC17	132.1mV
DEC18	134.5mV	DEC19	129.6mV	DEC20	132.1mV
DEC21	129.6mV	DEC22	129.6mV	DEC23	132.1mV
DEC24	127.2mV	DEC25	132.1mV	DEC26	132.1mV
DEC27	132.1mV	DEC28	132.1mV	DEC29	127.2mV
DEC30	139.4mV	DEC31	129.6mV	DEC32	134.5mV
DEC33	134.5mV	DEC34	132.1mV	DEC35	137.0mV
DEC36	134.5mV	DEC37	134.5mV	DEC38	132.1mV
DEC39	134.5mV	MOUT40	132.1mV	MOUT41	134.5mV
MOUT42	134.5mV	MOUT43	137.0mV	MOUT44	132.1mV
MOUT45	129.6mV	MOUT46	134.5mV	MOUT47	137.0mV
DEC0B	129.6mV	DEC1B	132.1mV	DEC2B	132.1mV
DEC3B	134.5mV	DEC4B	134.5mV	DEC5B	129.6mV
DEC6B	129.6mV	DEC7B	132.1mV	DEC8B	134.5mV
DEC9B	132.1mV	DEC10B	132.1mV	DEC11B	132.1mV
DEC12B	134.5mV	DEC13B	134.5mV	DEC14B	134.5mV
DEC15B	134.5mV	DEC16B	134.5mV	DEC17B	132.1mV
DEC18B	129.6mV	DEC19B	132.1mV	DEC20B	132.1mV
DEC21B	129.6mV	DEC22B	149.2mV	DEC23B	137.0mV
DEC24B	129.6mV	DEC25B	132.1mV	DEC26B	132.1mV
DEC27B	129.6mV	DEC28B	132.1mV	DEC29B	129.6mV
DEC30B	129.6mV	DEC31B	129.6mV	DEC32B	132.1mV
DEC33B	134.5mV	DEC34B	132.1mV	DEC35B	137.0mV
DEC36B	134.5mV	DEC37B	139.4mV	DEC38B	137.0mV
DEC39B	132.1mV	OUT40B	132.1mV	OUT41B	132.1mV
OUT42B	139.4mV	OUT43B	134.5mV	OUT44B	134.5mV
OUT45B	134.5mV	OUT46B	134.5mV	OUT47B	132.1mV

VOL params: Vcc = 5.00V, Vih = 3.000V, Vil = 0.000V, Io = 6.000mA.
Limits: 0.000 V minimum, 400.0mV maximum.

Q0	129.6mV	Q1	127.2mV	Q2	127.2mV
Q3	129.6mV	Q0B	129.6mV	Q1B	132.1mV
Q2B	129.6mV	Q3B	134.5mV	TOUTA	132.1mV
QOUTA	132.1mV	TOUTB	129.6mV	QOUTB	132.1mV
MKTOUT	132.1mV	MKOUTB	132.1mV	MMOUT	132.1mV
COUT	132.1mV	P0	127.2mV	P1	129.6mV
P2	127.2mV	P3	141.9mV	P4	124.8mV
P5	127.2mV	P6	129.6mV	P7	124.8mV
DEC0	127.2mV	DEC1	132.1mV	DEC2	129.6mV
DEC3	127.2mV	DEC4	129.6mV	DEC5	132.1mV
DEC6	127.2mV	DEC7	132.1mV	DEC8	151.7mV
DEC9	124.8mV	DEC10	124.8mV	DEC11	127.2mV
DEC12	127.2mV	DEC13	149.2mV	DEC14	132.1mV
DEC15	134.5mV	DEC16	127.2mV	DEC17	127.2mV
DEC18	129.6mV	DEC19	124.8mV	DEC20	127.2mV
DEC21	127.2mV	DEC22	127.2mV	DEC23	127.2mV
DEC24	124.8mV	DEC25	129.6mV	DEC26	127.2mV
DEC27	127.2mV	DEC28	127.2mV	DEC29	124.8mV
DEC30	134.5mV	DEC31	127.2mV	DEC32	129.6mV
DEC33	132.1mV	DEC34	127.2mV	DEC35	132.1mV
DEC36	132.1mV	DEC37	129.6mV	DEC38	127.2mV
DEC39	132.1mV	MOUT40	127.2mV	MOUT41	129.6mV
MOUT42	129.6mV	MOUT43	132.1mV	MOUT44	127.2mV
MOUT45	127.2mV	MOUT46	129.6mV	MOUT47	132.1mV
DEC0B	124.8mV	DEC1B	127.2mV	DEC2B	124.8mV

DEC3B	132.1mV	DEC4B	129.6mV	DEC5B	127.2mV
DEC6B	124.8mV	DEC7B	129.6mV	DEC8B	129.6mV
DEC9B	129.6mV	DEC10B	129.6mV	DEC11B	129.6mV
DEC12B	129.6mV	DEC13B	129.6mV	DEC14B	129.6mV
DEC15B	129.6mV	DEC16B	129.6mV	DEC17B	127.2mV
DEC18B	127.2mV	DEC19B	127.2mV	DEC20B	129.6mV
DEC21B	124.8mV	DEC22B	146.8mV	DEC23B	132.1mV
DEC24B	127.2mV	DEC25B	129.6mV	DEC26B	129.6mV
DEC27B	127.2mV	DEC28B	127.2mV	DEC29B	127.2mV
DEC30B	124.8mV	DEC31B	124.8mV	DEC32B	129.6mV
DEC33B	129.6mV	DEC34B	127.2mV	DEC35B	134.5mV
DEC36B	132.1mV	DEC37B	134.5mV	DEC38B	134.5mV
DEC39B	127.2mV	OUT40B	129.6mV	OUT41B	127.2mV
OUT42B	134.5mV	OUT43B	129.6mV	OUT44B	129.6mV
OUT45B	129.6mV	OUT46B	129.6mV	OUT47B	127.2mV

VOL params: Vcc = 5.25V, Vih = 3.000V, Vil = 0.000V, Io = 6.000mA.
Limits: 0.000 V minimum, 400.0mV maximum.

Q0	124.8mV	Q1	124.8mV	Q2	124.8mV
Q3	127.2mV	Q0B	124.8mV	Q1B	127.2mV
Q2B	124.8mV	Q3B	129.6mV	TOUTA	127.2mV
QOUTA	129.6mV	TOUTB	127.2mV	QOUTB	129.6mV
MKTOUT	127.2mV	MKOUTB	127.2mV	MMOUT	127.2mV
COUT	127.2mV	P0	124.8mV	P1	124.8mV
P2	124.8mV	P3	137.0mV	P4	122.3mV
P5	124.8mV	P6	124.8mV	P7	124.8mV
DEC0	124.8mV	DEC1	129.6mV	DEC2	127.2mV
DEC3	124.8mV	DEC4	124.8mV	DEC5	129.6mV
DEC6	124.8mV	DEC7	127.2mV	DEC8	146.8mV
DEC9	122.3mV	DEC10	119.9mV	DEC11	122.3mV
DEC12	124.8mV	DEC13	144.3mV	DEC14	129.6mV
DEC15	132.1mV	DEC16	124.8mV	DEC17	122.3mV
DEC18	124.8mV	DEC19	122.3mV	DEC20	124.8mV
DEC21	124.8mV	DEC22	124.8mV	DEC23	124.8mV
DEC24	119.9mV	DEC25	124.8mV	DEC26	124.8mV
DEC27	124.8mV	DEC28	122.3mV	DEC29	122.3mV
DEC30	129.6mV	DEC31	122.3mV	DEC32	124.8mV
DEC33	129.6mV	DEC34	122.3mV	DEC35	129.6mV
DEC36	127.2mV	DEC37	127.2mV	DEC38	124.8mV
DEC39	129.6mV	MOUT40	124.8mV	MOUT41	127.2mV
MOUT42	127.2mV	MOUT43	129.6mV	MOUT44	124.8mV
MOUT45	122.3mV	MOUT46	124.8mV	MOUT47	129.6mV
DEC0B	122.3mV	DEC1B	124.8mV	DEC2B	122.3mV
DEC3B	127.2mV	DEC4B	127.2mV	DEC5B	122.3mV
DEC6B	122.3mV	DEC7B	124.8mV	DEC8B	127.2mV
DEC9B	124.8mV	DEC10B	124.8mV	DEC11B	127.2mV
DEC12B	127.2mV	DEC13B	124.8mV	DEC14B	127.2mV
DEC15B	124.8mV	DEC16B	127.2mV	DEC17B	124.8mV
DEC18B	124.8mV	DEC19B	124.8mV	DEC20B	124.8mV
DEC21B	124.8mV	DEC22B	141.9mV	DEC23B	129.6mV
DEC24B	122.3mV	DEC25B	124.8mV	DEC26B	127.2mV
DEC27B	124.8mV	DEC28B	124.8mV	DEC29B	122.3mV
DEC30B	122.3mV	DEC31B	122.3mV	DEC32B	124.8mV
DEC33B	127.2mV	DEC34B	124.8mV	DEC35B	129.6mV
DEC36B	129.6mV	DEC37B	129.6mV	DEC38B	129.6mV
DEC39B	124.8mV	OUT40B	127.2mV	OUT41B	124.8mV
OUT42B	132.1mV	OUT43B	127.2mV	OUT44B	124.8mV
OUT45B	124.8mV	OUT46B	127.2mV	OUT47B	124.8mV

VOL params: Vcc = 5.50V, Vih = 3.000V, Vil = 0.000V, Io = 6.000mA.
Limits: 0.000 V minimum, 400.0mV maximum.

Q0	122.3mV	Q1	119.9mV	Q2	122.3mV
Q3	122.3mV	Q0B	124.8mV	Q1B	124.8mV
Q2B	119.9mV	Q3B	124.8mV	TOUTA	124.8mV
QOUTA	127.2mV	TOUTB	124.8mV	QOUTB	124.8mV
MKTOUT	124.8mV	MKOUTB	124.8mV	MMOUT	124.8mV
COUT	124.8mV	P0	119.9mV	P1	124.8mV
P2	119.9mV	P3	134.5mV	P4	119.9mV
P5	122.3mV	P6	122.3mV	P7	119.9mV
DEC0	122.3mV	DEC1	127.2mV	DEC2	122.3mV
DEC3	119.9mV	DEC4	124.8mV	DEC5	127.2mV
DEC6	122.3mV	DEC7	124.8mV	DEC8	144.3mV
DEC9	119.9mV	DEC10	119.9mV	DEC11	119.9mV
DEC12	122.3mV	DEC13	144.3mV	DEC14	127.2mV
DEC15	127.2mV	DEC16	119.9mV	DEC17	119.9mV
DEC18	122.3mV	DEC19	117.4mV	DEC20	119.9mV
DEC21	119.9mV	DEC22	119.9mV	DEC23	122.3mV
DEC24	117.4mV	DEC25	122.3mV	DEC26	122.3mV
DEC27	122.3mV	DEC28	119.9mV	DEC29	119.9mV
DEC30	127.2mV	DEC31	119.9mV	DEC32	122.3mV
DEC33	124.8mV	DEC34	119.9mV	DEC35	124.8mV
DEC36	124.8mV	DEC37	124.8mV	DEC38	122.3mV
DEC39	124.8mV	MOUT40	122.3mV	MOUT41	124.8mV
MOUT42	124.8mV	MOUT43	124.8mV	MOUT44	122.3mV
MOUT45	122.3mV	MOUT46	124.8mV	MOUT47	124.8mV
DEC0B	119.9mV	DEC1B	122.3mV	DEC2B	122.3mV
DEC3B	124.8mV	DEC4B	122.3mV	DEC5B	119.9mV
DEC6B	119.9mV	DEC7B	122.3mV	DEC8B	124.8mV
DEC9B	124.8mV	DEC10B	122.3mV	DEC11B	122.3mV
DEC12B	122.3mV	DEC13B	124.8mV	DEC14B	122.3mV
DEC15B	122.3mV	DEC16B	124.8mV	DEC17B	119.9mV
DEC18B	119.9mV	DEC19B	119.9mV	DEC20B	119.9mV
DEC21B	119.9mV	DEC22B	139.4mV	DEC23B	124.8mV
DEC24B	119.9mV	DEC25B	122.3mV	DEC26B	122.3mV
DEC27B	119.9mV	DEC28B	122.3mV	DEC29B	119.9mV
DEC30B	119.9mV	DEC31B	119.9mV	DEC32B	122.3mV
DEC33B	124.8mV	DEC34B	122.3mV	DEC35B	127.2mV
DEC36B	124.8mV	DEC37B	127.2mV	DEC38B	127.2mV
DEC39B	119.9mV	OUT40B	124.8mV	OUT41B	119.9mV
OUT42B	129.6mV	OUT43B	124.8mV	OUT44B	122.3mV
OUT45B	122.3mV	OUT46B	122.3mV	OUT47B	122.3mV

isb params: Vcc = 4.50V, Ins=4.50V, Outs = OPEN.

isb	0.000	146.7u	25.00m	13	pass

isb params: Vcc = 4.75V, Ins=4.75V, Outs = OPEN.

isb	0.000	160.0u	25.00m	13	pass

isb params: Vcc = 5.00V, Ins=5.00V, Outs = OPEN.

isb	0.000	190.0u	25.00m	13	pass

isb params: Vcc = 5.25V, Ins=5.25V, Outs = OPEN.

isb	0.000	230.0u	25.00m	13	pass

isb params: Vcc = 5.50V, Ins=5.50V, Outs = OPEN.

isb	0.000	240.0u	25.00m	13	pass

iil params: Vcc = 4.50V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	-0.183nA	CLKB	0.061nA	NRESET	-0.061nA
NLOAD	0.000 A	SEL	-0.061nA	CMPSEL	0.000 A
ESEL	-0.183nA	PAB	0.061nA	TSE	0.000 A
MKTINA	0.000 A	MKTINB	0.000 A	EA0	0.000 A
EA1	-0.061nA	EA2	0.000 A	EA3	-0.061nA
Q0	-0.061nA	Q1	-0.122nA	Q2	-0.061nA
Q3	0.061nA	Q0B	-0.183nA	Q1B	-0.061nA
Q2B	-0.061nA	Q3B	0.000 A		

iil params: Vcc = 4.75V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.000 A	CLKB	0.061nA	NRESET	0.061nA
NLOAD	-0.122nA	SEL	0.000 A	CMPSEL	0.000 A
ESEL	-0.061nA	PAB	0.000 A	TSE	-0.061nA
MKTINA	-0.061nA	MKTINB	0.183nA	EA0	-0.061nA
EA1	0.000 A	EA2	0.000 A	EA3	-0.122nA
Q0	-0.183nA	Q1	-0.061nA	Q2	-0.061nA
Q3	-0.122nA	Q0B	-0.122nA	Q1B	-0.061nA
Q2B	0.000 A	Q3B	-0.061nA		

iil params: Vcc = 5.00V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.061nA	CLKB	0.061nA	NRESET	0.000 A
NLOAD	0.000 A	SEL	-0.061nA	CMPSEL	-0.122nA
ESEL	0.122nA	PAB	0.061nA	TSE	-0.122nA
MKTINA	0.000 A	MKTINB	0.000 A	EA0	-0.122nA
EA1	-0.122nA	EA2	0.000 A	EA3	-0.305nA
Q0	0.000 A	Q1	-0.366nA	Q2	-0.183nA
Q3	-0.122nA	Q0B	0.000 A	Q1B	0.000 A
Q2B	-0.122nA	Q3B	-0.122nA		

iil params: Vcc = 5.25V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	-0.061nA	CLKB	0.000 A	NRESET	0.000 A
NLOAD	-0.061nA	SEL	0.000 A	CMPSEL	0.000 A
ESEL	-0.122nA	PAB	0.061nA	TSE	0.000 A
MKTINA	0.000 A	MKTINB	0.000 A	EA0	-0.061nA
EA1	0.000 A	EA2	-0.061nA	EA3	0.000 A
Q0	-0.061nA	Q1	-0.061nA	Q2	-0.183nA
Q3	0.183nA	Q0B	-0.122nA	Q1B	0.000 A
Q2B	0.000 A	Q3B	0.000 A		

iil params: Vcc = 5.50V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.061nA	CLKB	-0.122nA	NRESET	-0.061nA
NLOAD	-0.305nA	SEL	-0.122nA	CMPSEL	0.000 A
ESEL	0.000 A	PAB	0.000 A	TSE	-0.122nA
MKTINA	-0.122nA	MKTINB	0.061nA	EA0	0.000 A
EA1	-0.122nA	EA2	0.000 A	EA3	0.000 A
Q0	-0.122nA	Q1	0.061nA	Q2	-0.061nA
Q3	0.000 A	Q0B	-0.183nA	Q1B	-0.122nA
Q2B	0.000 A	Q3B	-0.061nA		

iih params: Vcc = 4.50V, Vin = 4.50V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.305nA	CLKB	0.122nA	NRESET	0.183nA
NLOAD	0.061nA	SEL	0.183nA	CMPSEL	0.183nA
ESEL	0.061nA	PAB	0.244nA	TSE	0.000 A
MKTINA	0.122nA	MKTINB	0.061nA	EA0	0.488nA
EA1	0.000 A	EA2	0.244nA	EA3	-0.061nA
Q0	0.244nA	Q1	0.183nA	Q2	0.244nA
Q3	0.000 A	Q0E	0.427nA	Q1B	0.000 A
Q2B	0.183nA	Q3E	0.244nA		

iih params: Vcc = 4.75V, Vin = 4.75V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.244nA	CLKB	0.000 A	NRESET	0.061nA
NLOAD	0.244nA	SEL	0.061nA	CMPSEL	0.000 A
ESEL	0.000 A	PAB	0.183nA	TSE	0.244nA
MKTINA	0.061nA	MKTINB	0.061nA	EA0	0.305nA
EA1	0.061nA	EA2	0.061nA	EA3	0.061nA
Q0	0.305nA	Q1	0.244nA	Q2	0.244nA
Q3	0.061nA	Q0E	0.244nA	Q1B	-0.061nA
Q2B	0.000 A	Q3E	0.122nA		

iih params: Vcc = 5.00V, Vin = 5.00V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.427nA	CLKB	0.122nA	NRESET	0.000 A
NLOAD	0.122nA	SEL	-0.122nA	CMPSEL	0.061nA
ESEL	0.122nA	PAB	0.244nA	TSE	0.061nA
MKTINA	0.061nA	MKTINB	0.000 A	EA0	0.366nA
EA1	0.000 A	EA2	-0.061nA	EA3	0.000 A
Q0	0.183nA	Q1	0.244nA	Q2	0.244nA
Q3	0.122nA	Q0E	0.366nA	Q1B	0.000 A
Q2B	0.061nA	Q3E	0.122nA		

iih params: Vcc = 5.25V, Vin = 5.25V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.549nA	CLKB	0.000 A	NRESET	0.000 A
NLOAD	0.061nA	SEL	0.000 A	CMPSEL	-0.061nA
ESEL	0.244nA	PAB	0.122nA	TSE	0.305nA
MKTINA	0.122nA	MKTINB	0.366nA	EA0	0.305nA
EA1	0.061nA	EA2	0.000 A	EA3	0.122nA
Q0	0.122nA	Q1	0.488nA	Q2	0.305nA
Q3	0.061nA	Q0E	0.610nA	Q1B	0.122nA
Q2B	0.061nA	Q3E	0.183nA		

iih params: Vcc = 5.50V, Vin = 5.50V
Limits: -10.000uA minimum, 10.000uA maximum.

CLKA	0.486nA	CLKB	0.061nA	NRESET	0.000 A
NLOAD	0.183nA	SEL	0.183nA	CMPSEL	0.061nA
ESEL	0.183nA	PAB	0.122nA	TSE	0.061nA
MKTINA	0.061nA	MKTINB	0.366nA	EA0	0.244nA
EA1	0.122nA	EA2	0.061nA	EA3	0.000 A
Q0	0.244nA	Q1	0.305nA	Q2	0.366nA
Q3	0.183nA	Q0E	0.305nA	Q1B	-0.061nA
Q2B	0.061nA	Q3E	0.244nA		

JPL Beta-12 A128C FPGA Temp: 25 Ser #: 3
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Source file: Beta12.C:H44
Post 500 hrs

iozl params: Vcc = 4.50V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	0.000 A	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.000 A	Q1B	0.000 A
Q2B	0.000 A	Q3B	-0.610nA	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.000 A	QOUTB	0.000 A
MKTOUT	1.829nA	MKOUTB	-0.610nA	MMOUT	0.000 A
COUT	0.000 A	P0	0.610nA	P1	1.829nA
P2	0.000 A	P3	2.439nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	-0.610nA	DEC2	0.000 A
DEC3	0.000 A	DEC4	0.000 A	DEC5	0.000 A
DEC6	-1.220nA	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.000 A	DEC10	0.000 A	DEC11	-0.610nA
DEC12	0.000 A	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.610nA	DEC16	1.829nA	DEC17	-0.610nA
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	0.000 A	DEC28	0.610nA	DEC29	0.000 A
DEC30	0.610nA	DEC31	0.000 A	DEC32	0.000 A
DEC33	0.000 A	DEC34	0.000 A	DEC35	1.829nA
DEC36	1.829nA	DEC37	0.000 A	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.000 A
MOUT42	1.829nA	MOUT43	0.000 A	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	-0.610nA
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	0.000 A
DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	-0.610nA	DEC8B	0.000 A
DEC9B	-0.610nA	DEC10B	0.000 A	DEC11B	0.000 A
DEC12B	-0.610nA	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	-0.610nA	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.000 A	DEC20B	0.000 A
DEC21B	1.829nA	DEC22B	0.000 A	DEC23B	0.000 A
DEC24B	-0.610nA	DEC25B	0.000 A	DEC26B	-0.610nA
DEC27B	0.000 A	DEC28B	0.000 A	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.000 A	DEC32B	0.000 A
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.610nA
DEC36B	0.610nA	DEC37B	0.000 A	DEC38B	0.000 A
DEC39B	0.000 A	OUT40B	1.829nA	OUT41B	1.829nA
OUT42B	0.000 A	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.000 A

iozl params: Vcc = 4.75V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	-0.610nA	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.000 A	Q1B	0.000 A
Q2B	0.000 A	Q3B	0.000 A	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.000 A	QOUTB	0.000 A
MKTOUT	1.829nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.000 A	P1	1.829nA
P2	0.000 A	P3	1.829nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	0.000 A	DEC2	0.000 A

DEC3	0.000 A	DEC4	0.000 A	DEC5	0.000 A
DEC6	0.000 A	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.000 A	DEC10	0.000 A	DEC11	-1.220nA
DEC12	-0.610nA	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.000 A	DEC16	1.829nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	2.439nA	DEC22	0.000 A	DEC23	-0.610nA
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	-0.610nA	DEC28	0.000 A	DEC29	0.000 A
DEC30	0.610nA	DEC31	0.000 A	DEC32	0.000 A
DEC33	0.000 A	DEC34	0.000 A	DEC35	1.829nA
DEC36	2.439nA	DEC37	0.000 A	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	-0.610nA
MOUT42	1.829nA	MOUT43	0.000 A	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	0.000 A
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	-0.610nA
DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	-0.610nA
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.000 A
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.610nA
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	0.000 A	DEC16B	-0.610nA	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.000 A	DEC20B	0.000 A
DEC21B	1.829nA	DEC22B	0.000 A	DEC23B	0.000 A
DEC24B	0.000 A	DEC25B	0.000 A	DEC26B	0.000 A
DEC27B	0.000 A	DEC28B	0.000 A	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.000 A	DEC32B	0.610nA
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.000 A
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.000 A	OUT40B	1.220nA	OUT41B	1.829nA
OUT42B	0.000 A	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.000 A

iozl params: Vcc = 5.00V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	-1.220nA	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.000 A	Q1B	0.000 A
Q2B	0.000 A	Q3B	-0.610nA	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.000 A	QOUTB	0.610nA
MKTOUT	1.220nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.000 A	P1	1.220nA
P2	0.000 A	P3	1.829nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	0.000 A	DEC2	-0.610nA
DEC3	0.000 A	DEC4	0.000 A	DEC5	0.000 A
DEC6	-0.610nA	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.000 A	DEC10	0.000 A	DEC11	-0.610nA
DEC12	0.000 A	DEC13	0.000 A	DEC14	0.610nA
DEC15	0.610nA	DEC16	1.829nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	0.610nA	DEC28	0.610nA	DEC29	0.000 A
DEC30	0.000 A	DEC31	0.000 A	DEC32	0.000 A
DEC33	0.000 A	DEC34	0.000 A	DEC35	1.829nA
DEC36	1.829nA	DEC37	0.000 A	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.000 A
MOUT42	1.220nA	MOUT43	0.000 A	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	-0.610nA
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	-0.610nA

DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	-1.220nA
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.000 A
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	0.000 A	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.000 A	DEC20B	0.610nA
DEC21B	1.829nA	DEC22B	0.000 A	DEC23B	0.610nA
DEC24B	0.000 A	DEC25B	0.000 A	DEC26B	0.000 A
DEC27B	-0.610nA	DEC28B	0.000 A	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.000 A	DEC32B	0.000 A
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.000 A
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.000 A	OUT40B	1.220nA	OUT41B	2.439nA
OUT42B	0.610nA	OUT43B	0.000 A	OUT44B	0.610nA
OUT45B	0.610nA	OUT46B	0.000 A	OUT47B	0.000 A

iozl params: Vcc = 5.25V, Vin = 0.0CV
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	-0.610nA	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.610nA	Q1B	0.000 A
Q2B	0.000 A	Q3B	0.000 A	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.000 A	QOUTB	0.000 A
MKTOUT	1.829nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.000 A	P1	1.829nA
P2	0.000 A	P3	1.829nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	0.000 A	DEC2	0.000 A
DEC3	0.000 A	DEC4	0.000 A	DEC5	0.000 A
DEC6	0.000 A	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.000 A	DEC10	0.000 A	DEC11	-0.610nA
DEC12	0.000 A	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.000 A	DEC16	1.220nA	DEC17	-0.610nA
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	0.000 A	DEC28	0.000 A	DEC29	0.000 A
DEC30	0.000 A	DEC31	0.000 A	DEC32	0.000 A
DEC33	0.000 A	DEC34	0.610nA	DEC35	1.829nA
DEC36	1.829nA	DEC37	0.000 A	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.000 A
MOUT42	1.220nA	MOUT43	0.610nA	MOUT44	-0.610nA
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	0.000 A
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	0.000 A
DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	-0.610nA	DEC8B	0.000 A
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.000 A
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	1.220nA
DEC15B	0.000 A	DEC16B	0.000 A	DEC17B	-0.610nA
DEC18B	-0.610nA	DEC19B	0.000 A	DEC20B	0.000 A
DEC21B	1.829nA	DEC22B	0.610nA	DEC23B	0.000 A
DEC24B	0.000 A	DEC25B	0.000 A	DEC26B	0.000 A
DEC27B	-0.610nA	DEC28B	0.000 A	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.610nA	DEC32B	0.000 A
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.000 A
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.000 A	OUT40B	1.829nA	OUT41B	1.829nA
OUT42B	0.000 A	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.000 A

iozl params: Vcc = 5.50V, Vin = 0.00V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	-0.610nA	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.000 A	Q1B	0.000 A
Q2B	0.610nA	Q3B	0.000 A	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.610nA	QOUTB	0.610nA
MKTOUT	1.829nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.000 A	P1	2.439nA
P2	0.000 A	P3	1.829nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	-0.610nA	DEC2	0.610nA
DEC3	0.000 A	DEC4	0.000 A	DEC5	0.000 A
DEC6	-0.610nA	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.000 A	DEC10	0.000 A	DEC11	0.000 A
DEC12	0.000 A	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.000 A	DEC16	1.220nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	2.439nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	-1.220nA
DEC27	0.000 A	DEC28	0.000 A	DEC29	0.000 A
DEC30	0.000 A	DEC31	0.000 A	DEC32	0.000 A
DEC33	0.000 A	DEC34	0.610nA	DEC35	1.829nA
DEC36	1.220nA	DEC37	0.610nA	DEC38	0.000 A
DEC39	0.000 A	MOUT40	-0.610nA	MOUT41	0.000 A
MOUT42	1.220nA	MOUT43	0.000 A	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	0.000 A
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	0.000 A
DEC3B	-0.610nA	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.000 A
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.610nA
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	-0.610nA	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.000 A	DEC20B	0.000 A
DEC21B	1.829nA	DEC22B	0.000 A	DEC23B	0.000 A
DEC24B	0.000 A	DEC25B	0.000 A	DEC26B	0.000 A
DEC27B	-0.610nA	DEC28B	0.000 A	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.000 A	DEC32B	0.000 A
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.000 A
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.000 A
DEC39B	0.000 A	OUT40B	1.829nA	OUT41B	1.220nA
OUT42B	0.000 A	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.000 A

iozh params: Vcc = 4.50V, Vin = 4.50V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	0.610nA	Q1	0.610nA	Q2	0.610nA
Q3	0.000 A	Q0B	1.220nA	Q1B	0.000 A
Q2B	0.610nA	Q3B	0.610nA	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.610nA	QOUTB	0.610nA
MKTOUT	1.829nA	MKOUTB	0.000 A	MMOUT	0.610nA
COUT	0.000 A	P0	0.000 A	P1	1.829nA
P2	0.610nA	P3	2.439nA	P4	0.000 A
P5	0.610nA	P6	0.610nA	P7	0.000 A
DEC0	0.000 A	DEC1	0.000 A	DEC2	0.000 A
DEC3	0.610nA	DEC4	0.000 A	DEC5	0.610nA
DEC6	-0.610nA	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.610nA	DEC10	0.000 A	DEC11	0.000 A
DEC12	0.000 A	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.000 A	DEC16	1.829nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	0.000 A	DEC28	0.000 A	DEC29	0.000 A
DEC30	0.000 A	DEC31	0.610nA	DEC32	0.610nA
DEC33	0.000 A	DEC34	0.610nA	DEC35	2.439nA
DEC36	2.439nA	DEC37	0.610nA	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.610nA
MOUT42	1.220nA	MOUT43	0.610nA	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	0.000 A
DEC0B	0.000 A	DEC1B	0.610nA	DEC2B	0.000 A
DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.000 A
DEC9B	0.610nA	DEC10B	0.000 A	DEC11B	0.000 A
DEC12B	-0.610nA	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	0.000 A	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.000 A	DEC20B	0.000 A
DEC21B	1.829nA	DEC22B	0.000 A	DEC23B	0.610nA
DEC24B	-0.610nA	DEC25B	-0.610nA	DEC26B	0.000 A
DEC27B	0.000 A	DEC28B	1.220nA	DEC29B	-0.610nA
DEC30B	0.000 A	DEC31B	0.000 A	DEC32B	0.610nA
DEC33B	0.000 A	DEC34B	0.000 A	DEC35B	0.610nA
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.000 A	OUT40B	1.829nA	OUT41B	2.439nA
OUT42B	0.610nA	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.000 A

iozh params: Vcc = 4.75V, Vin = 4.75V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	0.000 A	Q1	0.000 A	Q2	0.610nA
Q3	0.610nA	Q0B	0.610nA	Q1B	0.000 A
Q2B	0.000 A	Q3B	0.610nA	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.610nA	QOUTB	0.000 A
MKTOUT	2.439nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.610nA	P0	1.220nA	P1	1.829nA
P2	0.000 A	P3	1.829nA	P4	0.000 A
P5	0.610nA	P6	0.610nA	P7	0.000 A
DEC0	0.610nA	DEC1	0.610nA	DEC2	0.000 A

DEC3	0.610nA	DEC4	0.000 A	DEC5	0.000 A
DEC6	0.000 A	DEC7	0.610nA	DEC8	0.000 A
DEC9	0.610nA	DEC10	0.000 A	DEC11	0.000 A
DEC12	0.610nA	DEC13	0.000 A	DEC14	0.000 A
DEC15	0.610nA	DEC16	1.220nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	2.439nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	-0.610nA	DEC25	0.000 A	DEC26	-0.610nA
DEC27	0.610nA	DEC28	0.000 A	DEC29	0.000 A
DEC30	0.610nA	DEC31	0.000 A	DEC32	0.610nA
DEC33	0.000 A	DEC34	0.610nA	DEC35	2.439nA
DEC36	1.829nA	DEC37	0.610nA	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.610nA
MOUT42	1.829nA	MOUT43	0.610nA	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	-0.610nA
DEC0B	0.000 A	DEC1B	0.610nA	DEC2B	0.000 A
DEC3B	0.000 A	DEC4B	0.000 A	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.000 A
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.000 A
DEC12B	0.000 A	DEC13B	-0.610nA	DEC14B	0.610nA
DEC15B	0.000 A	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.610nA	DEC19B	0.610nA	DEC20B	0.000 A
DEC21B	2.439nA	DEC22B	0.610nA	DEC23B	0.000 A
DEC24B	0.610nA	DEC25B	0.000 A	DEC26B	0.000 A
DEC27B	0.000 A	DEC28B	1.220nA	DEC29B	0.000 A
DEC30B	0.610nA	DEC31B	0.000 A	DEC32B	0.610nA
DEC33B	0.610nA	DEC34B	0.000 A	DEC35B	0.000 A
DEC36B	0.000 A	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.000 A	OUT40B	2.439nA	OUT41B	2.439nA
OUT42B	0.610nA	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.610nA	OUT46B	0.000 A	OUT47B	0.000 A

iozh params: Vcc = 5.00V, Vin = 5.00V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	0.000 A	Q1	0.610nA	Q2	0.610nA
Q3	0.000 A	Q0B	0.610nA	Q1B	0.000 A
Q2B	0.610nA	Q3B	0.610nA	TOUTA	0.610nA
QOUTA	0.610nA	TOUTB	0.000 A	QOUTB	0.000 A
MKTOUT	2.439nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.610nA	P1	1.829nA
P2	0.610nA	P3	1.220nA	P4	1.220nA
P5	0.610nA	P6	0.000 A	P7	0.000 A
DEC0	0.000 A	DEC1	0.000 A	DEC2	0.000 A
DEC3	0.000 A	DEC4	0.610nA	DEC5	0.610nA
DEC6	-0.610nA	DEC7	0.000 A	DEC8	0.000 A
DEC9	0.610nA	DEC10	0.000 A	DEC11	0.000 A
DEC12	-0.610nA	DEC13	0.610nA	DEC14	0.000 A
DEC15	1.220nA	DEC16	1.829nA	DEC17	0.000 A
DEC18	0.000 A	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.610nA	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.610nA
DEC27	0.610nA	DEC28	0.000 A	DEC29	0.610nA
DEC30	0.610nA	DEC31	0.000 A	DEC32	0.610nA
DEC33	0.000 A	DEC34	0.610nA	DEC35	2.439nA
DEC36	2.439nA	DEC37	0.610nA	DEC38	0.000 A
DEC39	0.000 A	MOUT40	0.000 A	MOUT41	0.610nA
MOUT42	1.220nA	MOUT43	0.610nA	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	-0.610nA
DEC0B	0.000 A	DEC1B	0.610nA	DEC2B	0.000 A

DEC3B	0.000 A	DEC4B	0.610nA	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.610nA
DEC9B	0.000 A	DEC10B	0.000 A	DEC11B	0.610nA
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	0.610nA	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.610nA	DEC20B	0.000 A
DEC21B	2.439nA	DEC22B	0.610nA	DEC23B	0.000 A
DEC24B	0.610nA	DEC25B	0.610nA	DEC26B	0.000 A
DEC27B	0.000 A	DEC28B	0.610nA	DEC29B	0.000 A
DEC30B	0.610nA	DEC31B	0.000 A	DEC32B	0.610nA
DEC33B	0.610nA	DEC34B	0.000 A	DEC35B	0.610nA
DEC36B	0.610nA	DEC37B	0.000 A	DEC38B	0.610nA
DEC39B	0.610nA	OUT40B	1.829nA	OUT41B	2.439nA
OUT42B	0.000 A	OUT43B	0.000 A	OUT44B	0.000 A
OUT45B	0.000 A	OUT46B	0.000 A	OUT47B	0.610nA

iozh params: Vcc = 5.25V, Vin = 5.25V
Limits: -10.000uA minimum, 10.000uA maximum.

Q0	0.000 A	Q1	0.000 A	Q2	0.000 A
Q3	0.000 A	Q0B	0.610nA	Q1B	0.000 A
Q2B	0.610nA	Q3B	0.610nA	TOUTA	0.000 A
QOUTA	0.000 A	TOUTB	0.000 A	QOUTB	0.610nA
MKTOUT	2.439nA	MKOUTB	0.000 A	MMOUT	0.000 A
COUT	0.000 A	P0	0.000 A	P1	1.829nA
P2	0.000 A	P3	2.439nA	P4	0.000 A
P5	0.000 A	P6	0.000 A	P7	0.000 A
DEC0	0.610nA	DEC1	0.000 A	DEC2	0.000 A
DEC3	0.610nA	DEC4	0.000 A	DEC5	0.610nA
DEC6	0.000 A	DEC7	0.610nA	DEC8	0.610nA
DEC9	0.610nA	DEC10	0.000 A	DEC11	0.000 A
DEC12	0.000 A	DEC13	0.610nA	DEC14	0.000 A
DEC15	1.220nA	DEC16	1.829nA	DEC17	0.000 A
DEC18	0.610nA	DEC19	0.000 A	DEC20	0.000 A
DEC21	1.829nA	DEC22	0.000 A	DEC23	0.000 A
DEC24	0.000 A	DEC25	0.000 A	DEC26	0.000 A
DEC27	0.000 A	DEC28	0.610nA	DEC29	0.610nA
DEC30	0.000 A	DEC31	0.610nA	DEC32	2.439nA
DEC33	0.610nA	DEC34	0.000 A	DEC35	0.000 A
DEC36	1.829nA	DEC37	0.000 A	DEC38	0.000 A
DEC39	0.610nA	MOUT40	0.610nA	MOUT41	0.610nA
MOUT42	1.829nA	MOUT43	0.000 A	MOUT44	0.000 A
MOUT45	0.000 A	MOUT46	0.000 A	MOUT47	0.000 A
DEC0B	0.000 A	DEC1B	0.000 A	DEC2B	0.000 A
DEC3B	0.000 A	DEC4B	0.610nA	DEC5B	0.000 A
DEC6B	0.000 A	DEC7B	0.000 A	DEC8B	0.610nA
DEC9B	0.610nA	DEC10B	0.000 A	DEC11B	0.610nA
DEC12B	0.000 A	DEC13B	0.000 A	DEC14B	0.610nA
DEC15B	0.000 A	DEC16B	0.000 A	DEC17B	0.000 A
DEC18B	0.000 A	DEC19B	0.610nA	DEC20B	0.610nA
DEC21B	2.439nA	DEC22B	0.610nA	DEC23B	0.000 A
DEC24B	0.610nA	DEC25B	0.610nA	DEC26B	0.000 A
DEC27B	0.000 A	DEC28B	0.610nA	DEC29B	0.610nA
DEC30B	0.610nA	DEC31B	0.000 A	DEC32B	0.610nA
DEC33B	0.610nA	DEC34B	0.000 A	DEC35B	0.610nA
DEC36B	0.000 A	DEC37B	1.220nA	DEC38B	2.439nA
DEC39B	0.000 A	OUT40B	0.000 A	OUT41B	0.000 A
OUT42B	0.000 A	OUT43B	0.610nA	OUT44B	0.000 A
OUT45B		OUT46B		OUT47B	

```
iozn params: Vcc = 5.50V, Vin = 5.50V
Limits: -10.000uA minimum,  10.000uA maximum.
Q0          0.610nA     Q1          0.610nA     Q2          0.610nA
Q3          0.610nA     Q0B         0.610nA     Q1B         0.000 A
Q2B         0.610nA     Q3B         0.610nA     TOUTA       0.000 A
QOUTA       0.000 A     TOUTB       0.610nA     QOUTB       0.000 A
MKTOUT      2.439nA     MKOUTB      0.000 A     MMOUT       0.610nA
COUT        0.610nA     P0          0.000 A     P1          1.829nA
P2          0.610nA     P3          1.829nA     P4          0.000 A
P5          0.000 A     P6          0.000 A     P7          0.610nA
DEC0        0.000 A     DEC1        0.000 A     DEC2        0.000 A
DEC3        0.000 A     DEC4        0.000 A     DEC5        0.610nA
DEC6        0.000 A     DEC7        0.000 A     DEC8        0.000 A
DEC9        0.610nA     DEC10       0.000 A     DEC11       0.000 A
DEC12       0.610nA     DEC13       0.000 A     DEC14      -0.610nA
DEC15       0.610nA     DEC16       2.439nA     DEC17       0.000 A
DEC18       0.000 A     DEC19       0.000 A     DEC20       0.000 A
DEC21       2.439nA     DEC22       0.000 A     DEC23       0.000 A
DEC24      -0.610nA     DEC25       0.000 A     DEC26       0.000 A
DEC27      -0.610nA     DEC28       0.610nA     DEC29       0.000 A
DEC30       0.610nA     DEC31       0.000 A     DEC32       0.000 A
DEC33       0.000 A     DEC34       0.610nA     DEC35       2.439nA
DEC36       2.439nA     DEC37       0.000 A     DEC38       0.000 A
DEC39       0.000 A     MOUT40      0.610nA     MOUT41      0.000 A
MOUT42      1.220nA     MOUT43      0.610nA     MOUT44      0.000 A
MOUT45      0.000 A     MOUT46      0.000 A     MOUT47      0.610nA
DEC0B       0.610nA     DEC1B       0.610nA     DEC2B       0.000 A
DEC3B       0.000 A     DEC4B       0.000 A     DEC5B       0.000 A
DEC6B       0.610nA     DEC7B       0.000 A     DEC8B       0.610nA
DEC9B       0.000 A     DEC10B      0.000 A     DEC11B      0.610nA
DEC12B      0.000 A     DEC13B      0.000 A     DEC14B      0.610nA
DEC15B      0.000 A     DEC16B      0.610nA     DEC17B     -0.610nA
DEC18B      0.000 A     DEC19B      0.000 A     DEC20B      0.000 A
DEC21B      1.829nA     DEC22B      0.000 A     DEC23B      0.610nA
DEC24B      0.610nA     DEC25B      0.610nA     DEC26B      0.000 A
DEC27B      0.000 A     DEC28B      0.610nA     DEC29B      0.610nA
DEC30B      0.610nA     DEC31B      0.000 A     DEC32B      0.610nA
DEC33B      0.000 A     DEC34B      0.610nA     DEC35B      0.610nA
DEC36B      0.610nA     DEC37B     -0.610nA     DEC38B      0.610nA
DEC39B      0.000 A     OUT40B      1.220nA     OUT41B      1.829nA
OUT42B      0.610nA     OUT43B      0.000 A     OUT44B      0.000 A
OUT45B      0.610nA     OUT46B      0.000 A     OUT47B      0.000 A

Device PASSED all tests.
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vih params: Vcc = 4.50V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.359 V	CLKB	1.402 V	NRESET	1.334 V
NLOAD	1.333 V	SEL	1.311 V	CMPSEL	1.318 V
ESEL	1.323 V	PAB	1.311 V	TSE	1.326 V
MKTINA	1.292 V	MKTINB	1.279 V	EA0	1.336 V
EA1	1.349 V	EA2	1.315 V	EA3	1.313 V
Q0	1.291 V	Q1	1.339 V	Q2	1.333 V
Q3	1.330 V	Q0B	1.291 V	Q1B	1.330 V
Q2B	1.330 V	Q3B	1.321 V		

vih params: Vcc = 4.75V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.455 V	CLKB	1.455 V	NRESET	1.389 V
NLOAD	1.384 V	SEL	1.359 V	CMPSEL	1.368 V
ESEL	1.374 V	PAB	1.361 V	TSE	1.374 V
MKTINA	1.342 V	MKTINB	1.326 V	EA0	1.387 V
EA1	1.405 V	EA2	1.367 V	EA3	1.359 V
Q0	1.339 V	Q1	1.392 V	Q2	1.384 V
Q3	1.384 V	Q0B	1.339 V	Q1B	1.384 V
Q2B	1.384 V	Q3B	1.370 V		

vih params: Vcc = 5.00V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.477 V	CLKB	1.512 V	NRESET	1.501 V
NLOAD	1.455 V	SEL	1.408 V	CMPSEL	1.417 V
ESEL	1.425 V	PAB	1.409 V	TSE	1.424 V
MKTINA	1.395 V	MKTINB	1.384 V	EA0	1.437 V
EA1	1.455 V	EA2	1.412 V	EA3	1.412 V
Q0	1.387 V	Q1	1.440 V	Q2	1.436 V
Q3	1.433 V	Q0B	1.389 V	Q1B	1.433 V
Q2B	1.433 V	Q3B	1.421 V		

vih params: Vcc = 5.25V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.537 V	CLKB	1.583 V	NRESET	1.493 V
NLOAD	1.484 V	SEL	1.478 V	CMPSEL	1.465 V
ESEL	1.472 V	PAB	1.455 V	TSE	1.500 V
MKTINA	1.440 V	MKTINB	1.430 V	EA0	1.488 V
EA1	1.501 V	EA2	1.463 V	EA3	1.465 V
Q0	1.436 V	Q1	1.491 V	Q2	1.484 V
Q3	1.481 V	Q0B	1.436 V	Q1B	1.481 V
Q2B	1.481 V	Q3B	1.471 V		

vih params: Vcc = 5.50V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.589 V	CLKB	1.642 V	NRESET	1.544 V
NLOAD	1.534 V	SEL	1.501 V	CMPSEL	1.512 V
ESEL	1.522 V	PAB	1.499 V	TSE	1.522 V
MKTINA	1.488 V	MKTINB	1.475 V	EA0	1.537 V
EA1	1.547 V	EA2	1.512 V	EA3	1.519 V
Q0	1.484 V	Q1	1.540 V	Q2	1.534 V
Q3	1.529 V	Q0B	1.484 V	Q1B	1.528 V
Q2B	1.529 V	Q3B	1.519 V		

vil params: Vcc = 4.50V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.203 V	CLKB	1.210 V	NRESET	1.255 V
NLOAD	1.279 V	SEL	1.210 V	CMPSEL	1.233 V
ESEL	1.245 V	PAB	1.232 V	MKTINA	1.222 V
MKTINB	1.196 V	EA0	1.233 V	EA1	1.220 V
EA2	1.210 V	EA3	1.207 V	Q0	1.329 V
Q1	1.266 V	Q2	1.255 V	Q3	1.245 V
Q0B	1.324 V	Q1B	1.266 V	Q2B	1.258 V
Q3B	1.235 V				

vil params: Vcc = 4.75V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.241 V	CLKB	1.242 V	NRESET	1.299 V
NLOAD	1.321 V	SEL	1.257 V	CMPSEL	1.280 V
ESEL	1.291 V	PAB	1.274 V	MKTINA	1.273 V
MKTINB	1.235 V	EA0	1.279 V	EA1	1.269 V
EA2	1.257 V	EA3	1.252 V	Q0	1.380 V
Q1	1.317 V	Q2	1.307 V	Q3	1.293 V
Q0B	1.375 V	Q1B	1.314 V	Q2B	1.307 V
Q3B	1.283 V				

vil params: Vcc = 5.00V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.276 V	CLKB	1.273 V	NRESET	1.339 V
NLOAD	1.367 V	SEL	1.304 V	CMPSEL	1.327 V
ESEL	1.339 V	PAB	1.317 V	MKTINA	1.339 V
MKTINB	1.296 V	EA0	1.327 V	EA1	1.315 V
EA2	1.304 V	EA3	1.299 V	Q0	1.431 V
Q1	1.365 V	Q2	1.352 V	Q3	1.342 V
Q0B	1.424 V	Q1B	1.365 V	Q2B	1.355 V
Q3B	1.329 V				

vil params: Vcc = 5.25V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.311 V	CLKB	1.304 V	NRESET	1.390 V
NLOAD	1.415 V	SEL	1.349 V	CMPSEL	1.367 V
ESEL	1.386 V	PAB	1.358 V	MKTINA	1.392 V
MKTINB	1.386 V	EA0	1.373 V	EA1	1.361 V
EA2	1.349 V	EA3	1.342 V	Q0	1.479 V
Q1	1.414 V	Q2	1.400 V	Q3	1.387 V
Q0B	1.472 V	Q1B	1.411 V	Q2B	1.403 V
Q3B	1.375 V				

vil params: Vcc = 5.50V.
Limits: 800.0mV minimum, 2.000 V maximum.

CLKA	1.346 V	CLKB	1.334 V	NRESET	1.437 V
NLOAD	1.462 V	SEL	1.393 V	CMPSEL	1.414 V
ESEL	1.426 V	PAB	1.397 V	MKTINA	1.437 V
MKTINB	1.431 V	EA0	1.418 V	EA1	1.405 V
EA2	1.393 V	EA3	1.386 V	Q0	1.528 V
Q1	1.462 V	Q2	1.446 V	Q3	1.434 V
Q0B	1.521 V	Q1B	1.459 V	Q2B	1.452 V
Q3B	1.421 V				

Tpzl_tse params: Vcc = 4.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	57.07nS	QOUTA	56.86nS	TOUTB	56.71nS
QOUTB	56.62nS	MKTOUT	56.64nS	MKOUTB	58.20nS
MMOUT	57.32nS	COUT	46.38nS	P0	52.29nS
P1	40.00nS	P2	54.31nS	P3	57.56nS
P4	59.19nS	P5	57.46nS	P6	59.12nS
P7	57.24nS	DEC0	56.71nS	DEC1	61.32nS
DEC2	57.42nS	DEC3	48.36nS	DEC4	48.01nS
DEC5	60.50nS	DEC6	63.40nS	DEC7	56.43nS
DEC8	53.92nS	DEC9	49.39nS	DEC10	54.45nS
DEC11	54.02nS	DEC12	54.27nS	DEC13	48.57nS
DEC14	57.17nS	DEC15	54.41nS	DEC16	51.83nS
DEC17	52.80nS	DEC18	51.51nS	DEC19	51.79nS
DEC20	52.25nS	DEC21	51.36nS	DEC22	54.20nS
DEC23	51.51nS	DEC24	56.73nS	DEC25	57.46nS
DEC26	56.57nS	DEC27	59.33nS	DEC28	56.96nS
DEC29	56.68nS	DEC30	61.21nS	DEC31	56.15nS
DEC32	52.32nS	DEC33	55.23nS	DEC34	59.97nS
DEC35	54.20nS	DEC36	58.45nS	DEC37	54.13nS
DEC38	57.03nS	DEC39	46.87nS	MOUT40	49.00nS
MOUT41	50.66nS	MOUT42	48.50nS	MOUT43	49.85nS
MOUT44	45.60nS	MOUT45	49.32nS	MOUT46	51.72nS
MOUT47	50.13nS	DEC0B	57.17nS	DEC1B	57.99nS
DEC2B	60.47nS	DEC3B	59.33nS	DEC4B	60.18nS
DEC5B	60.75nS	DEC6B	50.73nS	DEC7B	60.40nS
DEC8B	54.91nS	DEC9B	48.04nS	DEC10B	54.27nS
DEC11B	53.74nS	DEC12B	54.02nS	DEC13B	54.02nS
DEC14B	56.54nS	DEC15B	52.11nS	DEC16B	57.95nS
DEC17B	57.60nS	DEC18B	56.78nS	DEC19B	57.14nS
DEC20B	57.21nS	DEC21B	57.10nS	DEC22B	59.48nS
DEC23B	57.21nS	DEC24B	57.35nS	DEC25B	59.09nS
DEC26B	43.64nS	DEC27B	56.29nS	DEC28B	56.36nS
DEC29B	56.76nS	DEC30B	56.94nS	DEC31B	56.75nS
DEC32B	54.91nS	DEC33B	56.36nS	DEC34B	52.78nS
DEC35B	53.81nS	DEC36B	53.74nS	DEC37B	54.02nS
DEC38B	57.10nS	DEC39B	52.64nS	OUT40B	49.78nS
OUT41B	46.45nS	OUT42B	49.49nS	OUT43B	48.64nS
OUT44B	45.70nS	OUT45B	49.14nS	OUT46B	51.01nS
OUT47B	48.89nS				

Tpzl_tse params: Vcc = 4.75V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	55.47nS	QOUTA	55.26nS	TOUTB	55.09nS
QOUTB	55.26nS	MKTOUT	55.47nS	MKOUTB	57.00nS
MMOUT	55.37nS	COUT	44.96nS	P0	51.16nS
P1	38.52nS	P2	52.86nS	P3	56.32nS
P4	57.71nS	P5	56.25nS	P6	57.81nS
P7	56.01nS	DEC0	55.47nS	DEC1	59.86nS
DEC2	56.18nS	DEC3	47.01nS	DEC4	46.66nS
DEC5	59.05nS	DEC6	61.78nS	DEC7	55.16nS
DEC8	52.64nS	DEC9	47.79nS	DEC10	53.21nS
DEC11	52.78nS	DEC12	53.00nS	DEC13	47.09nS
DEC14	55.51nS	DEC15	53.17nS	DEC16	50.70nS

DEC17	51.62nS	DEC18	50.38nS	DEC19	50.63nS
DEC20	51.16nS	DEC21	50.55nS	DEC22	52.68nS
DEC23	50.38nS	DEC24	55.47nS	DEC25	55.97nS
DEC26	55.26nS	DEC27	58.09nS	DEC28	55.72nS
DEC29	55.26nS	DEC30	59.62nS	DEC31	54.84nS
DEC32	50.98nS	DEC33	53.67nS	DEC34	58.63nS
DEC35	52.89nS	DEC36	57.07nS	DEC37	52.68nS
DEC38	55.23nS	DEC39	45.42nS	MOUT40	47.69nS
MOUT41	49.21nS	MOUT42	47.23nS	MOUT43	48.68nS
MOUT44	44.25nS	MOUT45	48.01nS	MOUT46	50.13nS
MOUT47	48.86nS	DEC0B	55.69nS	DEC1B	56.54nS
DEC2B	59.12nS	DEC3B	58.63nS	DEC4B	58.91nS
DEC5B	59.33nS	DEC6B	49.10nS	DEC7B	59.19nS
DEC8B	53.42nS	DEC9B	46.62nS	DEC10B	52.96nS
DEC11B	52.50nS	DEC12B	52.89nS	DEC13B	52.93nS
DEC14B	54.87nS	DEC15B	50.87nS	DEC16B	56.68nS
DEC17B	56.32nS	DEC18B	55.65nS	DEC19B	56.01nS
DEC20B	56.15nS	DEC21B	55.97nS	DEC22B	58.09nS
DEC23B	56.08nS	DEC24B	55.90nS	DEC25B	57.74nS
DEC26B	42.31nS	DEC27B	55.05nS	DEC28B	55.19nS
DEC29B	55.55nS	DEC30B	57.39nS	DEC31B	55.47nS
DEC32B	53.35nS	DEC33B	54.73nS	DEC34B	51.37nS
DEC35B	52.47nS	DEC36B	52.40nS	DEC37B	52.57nS
DEC38B	55.40nS	DEC39B	51.19nS	OUT40B	48.25nS
OUT41B	45.00nS	OUT42B	48.25nS	OUT43B	47.40nS
OUT44B	44.36nS	OUT45B	47.72nS	OUT46B	49.35nS
OUT47B	47.72nS				

Tpzl_tse params: Vcc = 5.00V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	54.02nS	QOUTA	53.86nS	TOUTB	53.70nS
QOUTB	53.81nS	MKTOUT	54.38nS	MKOUTB	56.01nS
MMOUT	53.74nS	COUT	43.69nS	P0	50.24nS
P1	37.24nS	P2	51.62nS	P3	55.26nS
P4	56.50nS	P5	55.16nS	P6	56.61nS
P7	55.19nS	DEC0	54.38nS	DEC1	58.63nS
DEC2	55.09nS	DEC3	46.06nS	DEC4	45.53nS
DEC5	58.20nS	DEC6	60.43nS	DEC7	54.06nS
DEC8	51.62nS	DEC9	46.59nS	DEC10	52.22nS
DEC11	51.69nS	DEC12	51.93nS	DEC13	45.99nS
DEC14	54.13nS	DEC15	52.08nS	DEC16	49.74nS
DEC17	50.48nS	DEC18	49.46nS	DEC19	49.70nS
DEC20	50.13nS	DEC21	49.49nS	DEC22	51.44nS
DEC23	49.42nS	DEC24	54.45nS	DEC25	54.77nS
DEC26	54.17nS	DEC27	57.07nS	DEC28	54.70nS
DEC29	54.02nS	DEC30	58.20nS	DEC31	53.81nS
DEC32	49.78nS	DEC33	52.25nS	DEC34	57.56nS
DEC35	51.69nS	DEC36	56.01nS	DEC37	51.51nS
DEC38	53.67nS	DEC39	44.25nS	MOUT40	46.66nS
MOUT41	47.97nS	MOUT42	46.20nS	MOUT43	47.65nS
MOUT44	43.16nS	MOUT45	46.94nS	MOUT46	48.75nS
MOUT47	47.83nS	DEC0B	54.45nS	DEC1B	55.30nS
DEC2B	58.13nS	DEC3B	57.67nS	DEC4B	57.88nS
DEC5B	58.20nS	DEC6B	47.62nS	DEC7B	58.06nS
DEC8B	52.18nS	DEC9B	45.42nS	DEC10B	51.93nS
DEC11B	51.55nS	DEC12B	51.79nS	DEC13B	51.76nS
DEC14B	53.53nS	DEC15B	49.81nS	DEC16B	55.62nS
DEC17B	55.33nS	DEC18B	54.77nS	DEC19B	55.16nS
DEC20B	55.30nS	DEC21B	55.12nS	DEC22B	56.78nS
DEC23B	55.23nS	DEC24B	54.70nS	DEC25B	56.57nS

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DEC26B	41.28nS	DEC27B	54.02nS	DEC28B	54.09nS
DEC29B	54.48nS	DEC30B	55.97nS	DEC31B	54.48nS
DEC32B	52.01nS	DEC33B	53.35nS	DEC34B	50.20nS
DEC35B	51.33nS	DEC36B	51.16nS	DEC37B	51.40nS
DEC38B	53.78nS	DEC39B	50.06nS	OUT40B	47.01nS
OUT41B	43.79nS	OUT42B	47.23nS	OUT43B	46.38nS
OUT44B	43.33nS	OUT45B	46.77nS	OUT46B	48.01nS
OUT47B	46.06nS				

Tpzl_tse params: Vcc = 5.25V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	52.86nS	QOUTA	52.64nS	TOUTB	52.47nS
QOUTB	52.65nS	MKTOUT	53.63nS	MKOUTB	55.19nS
MMOUT	52.47nS	COUT	42.77nS	P0	49.46nS
P1	36.22nS	P2	50.66nS	P3	54.45nS
P4	55.51nS	P5	54.41nS	P6	55.51nS
P7	54.41nS	DEC0	53.32nS	DEC1	57.49nS
DEC2	54.09nS	DEC3	45.00nS	DEC4	44.68nS
DEC5	57.07nS	DEC6	59.19nS	DEC7	52.93nS
DEC8	50.63nS	DEC9	45.49nS	DEC10	51.26nS
DEC11	50.80nS	DEC12	51.01nS	DEC13	45.00nS
DEC14	53.00nS	DEC15	51.19nS	DEC16	48.86nS
DEC17	49.53nS	DEC18	48.64nS	DEC19	48.86nS
DEC20	49.35nS	DEC21	48.75nS	DEC22	50.41nS
DEC23	48.50nS	DEC24	53.46nS	DEC25	53.70nS
DEC26	53.17nS	DEC27	56.04nS	DEC28	53.67nS
DEC29	53.24nS	DEC30	57.07nS	DEC31	52.89nS
DEC32	48.62nS	DEC33	51.05nS	DEC34	56.43nS
DEC35	50.63nS	DEC36	54.91nS	DEC37	50.45nS
DEC38	52.43nS	DEC39	43.19nS	MOUT40	45.78nS
MOUT41	47.01nS	MOUT42	45.32nS	MOUT43	46.66nS
MOUT44	42.24nS	MOUT45	46.06nS	MOUT46	47.62nS
MOUT47	46.91nS	DEC0B	53.35nS	DEC1B	54.20nS
DEC2B	57.14nS	DEC3B	56.64nS	DEC4B	56.82nS
DEC5B	57.24nS	DEC6B	46.45nS	DEC7B	57.10nS
DEC8B	51.10nS	DEC9B	44.39nS	DEC10B	50.98nS
DEC11B	50.39nS	DEC12B	50.91nS	DEC13B	50.91nS
DEC14B	52.32nS	DEC15B	48.32nS	DEC16B	54.66nS
DEC17B	54.46nS	DEC18B	53.92nS	DEC19B	54.38nS
DEC20B	54.46nS	DEC21B	54.31nS	DEC22B	55.72nS
DEC23B	54.41nS	DEC24B	53.67nS	DEC25B	55.58nS
DEC26B	40.39nS	DEC27B	53.03nS	DEC28B	53.17nS
DEC29B	53.46nS	DEC30B	54.32nS	DEC31B	53.39nS
DEC32B	50.77nS	DEC33B	52.15nS	DEC34B	49.17nS
DEC35B	50.31nS	DEC36B	50.20nS	DEC37B	50.31nS
DEC38B	52.47nS	DEC39B	49.10nS	OUT40B	46.06nS
OUT41B	42.70nS	OUT42B	46.24nS	OUT43B	45.46nS
OUT44B	42.31nS	OUT45B	45.81nS	OUT46B	46.87nS
OUT47B	45.78nS				

Tpzl_tse params: Vcc = 5.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	51.96nS	QOUTA	51.72nS	TOUTB	51.47nS
QOUTB	51.62nS	MKTOUT	52.78nS	MKOUTB	54.24nS
MMOUT	51.37nS	COUT	41.81nS	P0	48.75nS
P1	35.33nS	P2	49.70nS	P3	53.78nS
P4	54.59nS	P5	53.63nS	P6	54.59nS
P7	53.67nS	DEC0	52.47nS	DEC1	56.64nS
DEC2	53.07nS	DEC3	44.18nS	DEC4	43.79nS
DEC5	56.40nS	DEC6	58.20nS	DEC7	52.01nS

DEC8	49.85nS	DEC9	44.64nS	DEC10	50.41nS
DEC11	50.02nS	DEC12	50.24nS	DEC13	44.25nS
DEC14	52.04nS	DEC15	50.41nS	DEC16	48.15nS
DEC17	48.71nS	DEC18	47.90nS	DEC19	48.25nS
DEC20	48.61nS	DEC21	48.01nS	DEC22	49.53nS
DEC23	47.90nS	DEC24	52.57nS	DEC25	52.78nS
DEC26	52.25nS	DEC27	55.26nS	DEC28	52.75nS
DEC29	52.50nS	DEC30	56.11nS	DEC31	52.01nS
DEC32	47.97nS	DEC33	50.20nS	DEC34	55.47nS
DEC35	49.78nS	DEC36	54.06nS	DEC37	49.60nS
DEC38	51.33nS	DEC39	42.24nS	MOUT40	44.96nS
MOUT41	46.20nS	MOUT42	44.54nS	MOUT43	45.99nS
MOUT44	41.35nS	MOUT45	45.28nS	MOUT46	46.73nS
MOUT47	46.09nS	DEC0B	52.50nS	DEC1B	53.39nS
DEC2B	56.25nS	DEC3B	55.72nS	DEC4B	55.97nS
DEC5B	56.64nS	DEC6B	45.42nS	DEC7B	56.22nS
DEC8B	50.38nS	DEC9B	43.62nS	DEC10B	50.24nS
DEC11B	49.55nS	DEC12B	50.06nS	DEC13B	50.06nS
DEC14B	51.33nS	DEC15B	47.97nS	DEC16B	53.99nS
DEC17B	53.61nS	DEC18B	53.28nS	DEC19B	53.70nS
DEC20B	53.75nS	DEC21B	53.63nS	DEC22B	54.91nS
DEC23B	53.74nS	DEC24B	52.75nS	DEC25B	54.80nS
DEC26B	39.54nS	DEC27B	52.11nS	DEC28B	52.22nS
DEC29B	52.61nS	DEC30B	53.81nS	DEC31B	52.54nS
DEC32B	49.85nS	DEC33B	51.2enS	DEC34B	48.29nS
DEC35B	49.42nS	DEC36B	49.17nS	DEC37B	49.42nS
DEC38B	51.40nS	DEC39B	43.11nS	OUT40B	45.10nS
OUT41B	41.88nS	OUT42B	45.46nS	OUT43B	44.68nS
OUT44B	41.49nS	OUT45B	44.9enS	OUT46B	45.92nS
OUT47B	45.00nS				

Source file: Beta12.C:H44
Post 500 hrs

Tpzh_tse params: Vcc = 4.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	65.00nS	QOUTA	65.00nS	TOUTB	66.06nS
QOUTB	65.00nS	MKTOUT	71.79nS	MKOUTB	72.93nS
MMOUT	63.86nS	COUT	63.02nS	P0	67.30nS
P1	47.90nS	P2	62.27nS	P3	71.72nS
P4	67.23nS	P5	71.41nS	P6	67.90nS
P7	71.69nS	DEC0	71.76nS	DEC1	74.59nS
DEC2	72.57nS	DEC3	63.56nS	DEC4	63.26nS
DEC5	74.87nS	DEC6	72.08nS	DEC7	71.41nS
DEC8	68.57nS	DEC9	64.50nS	DEC10	69.56nS
DEC11	68.75nS	DEC12	69.07nS	DEC13	63.72nS
DEC14	66.77nS	DEC15	69.25nS	DEC16	67.19nS
DEC17	66.84nS	DEC18	66.52nS	DEC19	67.33nS
DEC20	67.55nS	DEC21	66.98nS	DEC22	63.97nS
DEC23	67.12nS	DEC24	71.76nS	DEC25	71.65nS
DEC26	71.44nS	DEC27	73.95nS	DEC28	72.25nS
DEC29	72.11nS	DEC30	70.20nS	DEC31	72.25nS
DEC32	68.43nS	DEC33	68.93nS	DEC34	75.19nS
DEC35	69.76nS	DEC36	73.39nS	DEC37	68.64nS
DEC38	66.56nS	DEC39	63.26nS	MOUT40	64.61nS
MOUT41	64.06nS	MOUT42	63.86nS	MOUT43	64.82nS
MOUT44	60.30nS	MOUT45	64.61nS	MOUT46	61.71nS
MOUT47	65.00nS	DEC0B	71.41nS	DEC1B	72.68nS
DEC2B	75.16nS	DEC3B	74.52nS	DEC4B	74.87nS
DEC5B	75.55nS	DEC6B	60.80nS	DEC7B	74.84nS
DEC8B	68.93nS	DEC9B	62.77nS	DEC10B	69.49nS
DEC11B	68.29nS	DEC12B	66.75nS	DEC13B	68.64nS
DEC14B	66.06nS	DEC15B	67.51nS	DEC16B	70.94nS
DEC17B	70.91nS	DEC18B	71.58nS	DEC19B	71.62nS
DEC20B	71.16nS	DEC21B	71.37nS	DEC22B	69.00nS
DEC23B	71.23nS	DEC24B	71.51nS	DEC25B	72.71nS
DEC26B	58.27nS	DEC27B	72.18nS	DEC28B	72.11nS
DEC29B	71.41nS	DEC30B	68.50nS	DEC31B	72.79nS
DEC32B	68.89nS	DEC33B	71.72nS	DEC34B	63.04nS
DEC35B	69.10nS	DEC36B	65.61nS	DEC37B	68.29nS
DEC38B	66.56nS	DEC39B	68.68nS	OUT40B	64.15nS
OUT41B	61.17nS	OUT42B	64.22nS	OUT43B	63.58nS
OUT44B	60.89nS	OUT45B	64.01nS	OUT46B	60.43nS
OUT47B	64.89nS				

Tpzh_tse params: Vcc = 4.75V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	62.73nS	QOUTA	62.73nS	TOUTB	63.51nS
QOUTB	62.73nS	MKTOUT	68.68nS	MKOUTB	69.95nS
MMOUT	61.81nS	COUT	59.62nS	P0	64.57nS
P1	42.80nS	P2	60.25nS	P3	68.71nS
P4	65.00nS	P5	68.68nS	P6	65.67nS
P7	66.75nS	DEC0	68.68nS	DEC1	71.69nS
DEC2	69.14nS	DEC3	60.68nS	DEC4	60.32nS
DEC5	71.83nS	DEC6	69.25nS	DEC7	68.29nS
DEC8	65.67nS	DEC9	61.32nS	DEC10	66.52nS
DEC11	66.10nS	DEC12	66.27nS	DEC13	60.71nS
DEC14	64.22nS	DEC15	66.27nS	DEC16	64.36nS
DEC17	64.15nS	DEC18	63.65nS	DEC19	64.54nS
DEC20	64.61nS	DEC21	64.22nS	DEC22	61.71nS

DEC23	64.08nS	DEC24	68.75nS	DEC25	68.71nS
DEC26	68.36nS	DEC27	71.12nS	DEC28	69.25nS
DEC29	68.68nS	DEC30	67.69nS	DEC31	69.14nS
DEC32	65.32nS	DEC33	65.92nS	DEC34	72.01nS
DEC35	66.59nS	DEC36	70.27nS	DEC37	65.74nS
DEC38	63.79nS	DEC39	59.30nS	MOUT40	61.32nS
MOUT41	61.53nS	MOUT42	60.39nS	MOUT43	62.02nS
MOUT44	57.60nS	MOUT45	61.60nS	MOUT46	59.05nS
MOUT47	62.13nS	DECOB	68.40nS	DEC1B	69.49nS
DEC2B	72.25nS	DEC3B	71.55nS	DEC4B	71.94nS
DEC5B	72.33nS	DEC6B	58.27nS	DEC7B	71.87nS
DEC8B	66.10nS	DEC9B	59.79nS	DEC10B	66.80nS
DEC11B	65.53nS	DEC12B	65.61nS	DEC13B	65.74nS
DEC14B	63.55nS	DEC15B	64.33nS	DEC16B	68.40nS
DEC17B	68.29nS	DEC18B	68.68nS	DEC19B	68.89nS
DEC20B	68.54nS	DEC21B	68.54nS	DEC22B	66.52nS
DEC23B	68.57nS	DEC24B	68.04nS	DEC25B	69.99nS
DEC26B	55.55nS	DEC27B	69.14nS	DEC28B	68.64nS
DEC29B	68.43nS	DEC30B	65.55nS	DEC31B	69.49nS
DEC32B	66.02nS	DEC33B	68.29nS	DEC34B	65.00nS
DEC35B	66.02nS	DEC36B	65.53nS	DEC37B	65.32nS
DEC38B	63.86nS	DEC39B	65.53nS	OUT40B	61.14nS
OUT41B	58.17nS	OUT42B	61.56nS	OUT43B	60.78nS
OUT44B	57.92nS	OUT45B	61.00nS	OUT46B	57.92nS
OUT47B	61.60nS				

Tpzh_tse params: Vcc = 5.00V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	60.47nS	QOUTA	60.47nS	TOUTB	61.17nS
QOUTB	60.47nS	MKTOUT	66.20nS	MKOUTB	67.58nS
MMOUT	59.69nS	COUT	56.93nS	P0	62.34nS
P1	59.86nS	P2	58.52nS	P3	66.56nS
P4	62.34nS	P5	66.45nS	P6	62.70nS
P7	66.56nS	DEC0	65.92nS	DEC1	69.14nS
DEC2	66.84nS	DEC3	58.41nS	DEC4	58.20nS
DEC5	69.49nS	DEC6	65.95nS	DEC7	65.74nS
DEC8	63.30nS	DEC9	58.95nS	DEC10	64.29nS
DEC11	63.76nS	DEC12	63.36nS	DEC13	58.48nS
DEC14	61.95nS	DEC15	64.01nS	DEC16	62.09nS
DEC17	62.00nS	DEC18	61.49nS	DEC19	62.34nS
DEC20	62.45nS	DEC21	61.99nS	DEC22	59.72nS
DEC23	61.86nS	DEC24	66.20nS	DEC25	66.31nS
DEC26	65.74nS	DEC27	68.71nS	DEC28	66.87nS
DEC29	66.17nS	DEC30	65.32nS	DEC31	66.66nS
DEC32	62.63nS	DEC33	63.48nS	DEC34	69.49nS
DEC35	64.16nS	DEC36	67.79nS	DEC37	63.19nS
DEC38	61.39nS	DEC39	56.71nS	MOUT40	58.98nS
MOUT41	59.19nS	MOUT42	58.77nS	MOUT43	59.69nS
MOUT44	55.47nS	MOUT45	59.23nS	MOUT46	57.00nS
MOUT47	60.15nS	DECOB	65.71nS	DEC1B	67.16nS
DEC2B	69.60nS	DEC3B	69.21nS	DEC4B	69.53nS
DEC5B	69.71nS	DEC6B	56.04nS	DEC7B	69.53nS
DEC8B	63.79nS	DEC9B	57.67nS	DEC10B	64.50nS
DEC11B	63.16nS	DEC12B	63.40nS	DEC13B	63.48nS
DEC14B	61.17nS	DEC15B	61.85nS	DEC16B	66.31nS
DEC17B	66.13nS	DEC18B	66.59nS	DEC19B	66.70nS
DEC20B	66.41nS	DEC21B	66.34nS	DEC22B	64.33nS
DEC23B	66.41nS	DEC24B	66.06nS	DEC25B	67.69nS
DEC26B	53.00nS	DEC27B	66.80nS	DEC28B	66.13nS
DEC29B	65.85nS	DEC30B	63.40nS	DEC31B	67.16nS
DEC32B	63.48nS	DEC33B	65.74nS	DEC34B	62.70nS

DEC35B	63.55nS	DEC36B	63.02nS	DEC37B	62.91nS
DEC38B	61.32nS	DEC39B	63.09nS	OUT40B	58.94nS
OUT41B	56.01nS	OUT42B	59.19nS	OUT43B	58.55nS
OUT44B	55.72nS	OUT45B	58.73nS	OUT46B	55.86nS
OUT47B	59.23nS				

Tpzh_tse params: Vcc = 5.25V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	58.17nS	QOUTA	57.35nS	TOUTB	58.66nS
QOUTB	55.00nS	MKTOUT	63.94nS	MKOUTB	65.46nS
MMOUT	54.80nS	COUT	54.98nS	P0	60.47nS
P1	58.25nS	P2	57.00nS	P3	64.61nS
P4	59.05nS	P5	64.40nS	P6	59.94nS
P7	64.60nS	DEC0	63.65nS	DEC1	66.87nS
DEC2	64.54nS	DEC3	56.40nS	DEC4	56.25nS
DEC5	66.90nS	DEC6	61.85nS	DEC7	63.48nS
DEC8	61.17nS	DEC9	57.17nS	DEC10	62.34nS
DEC11	61.60nS	DEC12	61.78nS	DEC13	56.78nS
DEC14	59.65nS	DEC15	62.06nS	DEC16	60.32nS
DEC17	60.11nS	DEC18	59.58nS	DEC19	60.43nS
DEC20	60.54nS	DEC21	60.11nS	DEC22	57.92nS
DEC23	60.06nS	DEC24	63.79nS	DEC25	63.94nS
DEC26	63.58nS	DEC27	66.66nS	DEC28	64.89nS
DEC29	64.08nS	DEC30	61.00nS	DEC31	64.57nS
DEC32	60.47nS	DEC33	61.32nS	DEC34	67.26nS
DEC35	62.00nS	DEC36	65.76nS	DEC37	61.10nS
DEC38	59.25nS	DEC39	54.87nS	MOUT40	57.07nS
MOUT41	56.93nS	MOUT42	56.68nS	MOUT43	57.63nS
MOUT44	53.56nS	MOUT45	57.24nS	MOUT46	52.01nS
MOUT47	58.27nS	DEC0B	63.51nS	DEC1B	64.89nS
DEC2B	66.87nS	DEC3B	66.37nS	DEC4B	67.23nS
DEC5B	67.20nS	DEC6B	49.74nS	DEC7B	67.26nS
DEC8B	61.63nS	DEC9B	55.76nS	DEC10B	62.27nS
DEC11B	61.03nS	DEC12B	61.39nS	DEC13B	61.46nS
DEC14B	58.34nS	DEC15B	59.79nS	DEC16B	64.15nS
DEC17B	64.04nS	DEC18B	64.61nS	DEC19B	64.40nS
DEC20B	64.15nS	DEC21B	64.54nS	DEC22B	60.86nS
DEC23B	64.43nS	DEC24B	63.83nS	DEC25B	65.39nS
DEC26B	50.66nS	DEC27B	64.57nS	DEC28B	63.94nS
DEC29B	63.40nS	DEC30B	60.78nS	DEC31B	65.17nS
DEC32B	61.32nS	DEC33B	63.76nS	DEC34B	60.57nS
DEC35B	61.32nS	DEC36B	60.89nS	DEC37B	60.68nS
DEC38B	58.84nS	DEC39B	61.03nS	OUT40B	57.07nS
OUT41B	53.99nS	OUT42B	57.07nS	OUT43B	56.61nS
OUT44B	53.81nS	OUT45B	56.66nS	OUT46B	54.02nS
OUT47B	57.35nS				

Tpzh_tse params: Vcc = 5.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

TOUTA	54.24nS	QOUTA	54.52nS	TOUTB	54.84nS
QOUTB	54.41nS	MKTOUT	61.21nS	MKOUTB	61.60nS
MMOUT	53.00nS	COUT	53.28nS	P0	58.91nS
P1	36.93nS	P2	51.93nS	P3	62.13nS
P4	57.24nS	P5	61.78nS	P6	57.67nS
P7	62.63nS	DEC0	61.60nS	DEC1	62.63nS
DEC2	61.60nS	DEC3	50.13nS	DEC4	49.42nS
DEC5	62.38nS	DEC6	60.18nS	DEC7	61.14nS
DEC8	59.09nS	DEC9	55.47nS	DEC10	60.08nS
DEC11	58.94nS	DEC12	59.51nS	DEC13	50.34nS
DEC14	55.79nS	DEC15	60.11nS	DEC16	58.52nS
DEC17	58.48nS	DEC18	58.00nS	DEC19	58.77nS
DEC20	56.87nS	DEC21	58.48nS	DEC22	52.43nS

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DEC23          58.41nS     DEC24          61.60nS     DEC25          60.54nS
DEC26          61.60nS     DEC27          62.34nS     DEC28          62.31nS
DEC29          62.31nS     DEC30          58.87nS     DEC31          62.63nS
DEC32          58.55nS     DEC33          58.24nS     DEC34          62.91nS
DEC35          60.08nS     DEC36          62.34nS     DEC37          58.91nS
DEC38          54.38nS     DEC39          53.28nS     MOUT40         54.45nS
MOUT41         53.88nS     MOUT42         54.13nS     MOUT43         55.26nS
MOUT44         46.94nS     MOUT45         53.10nS     MOUT46         50.02nS
MOUT47         56.40nS     DEC08          61.60nS     DEC18          62.06nS
DEC28          62.45nS     DEC38          62.31nS     DEC48          62.59nS
DEC58          63.44nS     DEC68          47.80nS     DEC78          63.40nS
DEC88          59.33nS     DEC98          49.14nS     DEC1C8         59.69nS
DEC118         58.55nS     DEC128         59.33nS     DEC138         59.12nS
DEC148         55.16nS     DEC158         58.06nS     DEC168         60.93nS
DEC178         60.93nS     DEC188         61.60nS     DEC198         61.03nS
DEC208         61.60nS     DEC218         61.60nS     DEC228         58.48nS
DEC238         61.60nS     DEC248         61.39nS     DEC258         61.35nS
DEC268         44.78nS     DEC278         61.63nS     DEC288         62.17nS
DEC298         61.21nS     DEC308         57.46nS     DEC318         63.02nS
DEC328         59.19nS     DEC338         61.71nS     DEC348         58.38nS
DEC358         58.98nS     DEC368         56.68nS     DEC378         56.68nS
DEC388         54.34nS     DEC398         59.05nS     OUT4C8         53.10nS
OUT418         51.97nS     OUT428         54.53nS     OUT438         52.54nS
OUT448         51.93nS     OUT458         53.07nS     OUT468         48.39nS
OUT478         54.87nS
Device PASSED all tests.
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Tplhck params: Vcc = 4.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 2CC.0nS maximum.

Q0	31.20nS	Q1	35.74nS	Q2	33.02nS
Q3	36.52nS	Q0B	33.93nS	Q1B	36.94nS
Q2B	34.66nS	Q3B	33.38nS	TOUTA	30.22nS
QOUTA	17.40nS	TOUTB	28.95nS	QOUTB	17.33nS
MKTOUT	21.66nS	MKOUTB	21.63nS	MMOUT	70.37nS
COUT	70.19nS	P0	65.89nS	P1	84.15nS
P2	93.85nS	P3	107.7nS	P4	107.9nS
P5	133.2nS	P6	142.9nS	P7	131.4nS
DEC0	63.42nS	DEC1	65.50nS	DEC2	60.10nS
DEC3	64.56nS	DEC4	69.34nS	DEC5	63.97nS
DEC6	59.61nS	DEC7	61.53nS	DEC8	53.85nS
DEC9	54.97nS	DEC10	60.00nS	DEC11	53.31nS
DEC12	53.96nS	DEC13	56.08nS	DEC14	58.83nS
DEC15	54.47nS	DEC16	60.31nS	DEC17	61.01nS
DEC18	59.84nS	DEC19	60.80nS	DEC20	58.70nS
DEC21	60.06nS	DEC22	55.98nS	DEC23	59.95nS
DEC24	66.17nS	DEC25	68.87nS	DEC26	62.15nS
DEC27	69.34nS	DEC28	69.34nS	DEC29	62.41nS
DEC30	66.56nS	DEC31	70.94nS	DEC32	71.67nS
DEC33	68.25nS	DEC34	77.38nS	DEC35	69.67nS
DEC36	69.80nS	DEC37	74.91nS	DEC38	69.65nS
DEC39	69.34nS	MOUT40	86.02nS	MOUT41	87.65nS
MOUT42	81.68nS	MOUT43	79.58nS	MOUT44	74.06nS
MOUT45	76.13nS	MOUT46	79.87nS	MOUT47	74.91nS
DEC0B	59.01nS	DEC1B	61.61nS	DEC2B	61.68nS
DEC3B	58.86nS	DEC4B	58.54nS	DEC5B	58.57nS
DEC6B	61.45nS	DEC7B	60.85nS	DEC8B	50.97nS
DEC9B	52.22nS	DEC10B	53.98nS	DEC11B	54.89nS
DEC12B	50.40nS	DEC13B	51.85nS	DEC14B	51.57nS
DEC15B	60.70nS	DEC16B	60.21nS	DEC17B	58.29nS
DEC18B	58.54nS	DEC19B	58.83nS	DEC20B	56.34nS
DEC21B	58.54nS	DEC22B	58.60nS	DEC23B	55.77nS
DEC24B	61.32nS	DEC25B	53.07nS	DEC26B	52.81nS
DEC27B	54.73nS	DEC28B	61.61nS	DEC29B	58.73nS
DEC30B	52.99nS	DEC31B	56.34nS	DEC32B	58.47nS
DEC33B	59.95nS	DEC34B	58.29nS	DEC35B	58.86nS
DEC36B	58.83nS	DEC37B	57.92nS	DEC38B	55.20nS
DEC39B	60.78nS	OUT40B	80.72nS	OUT41B	66.59nS
OUT42B	74.60nS	OUT43B	77.17nS	OUT44B	79.87nS
OUT45B	75.72nS	OUT46B	70.58nS	OUT47B	75.74nS

Tplhck params: Vcc = 4.75V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	29.73nS	Q1	34.21nS	Q2	32.01nS
Q3	34.39nS	Q0B	32.53nS	Q1B	35.35nS
Q2B	33.23nS	Q3B	31.72nS	TOUTA	28.95nS
QOUTA	16.44nS	TOUTB	27.73nS	QOUTB	16.39nS
MKTOUT	20.72nS	MKOUTB	20.70nS	MMOUT	67.57nS
COUT	67.42nS	P0	63.60nS	P1	81.45nS
P2	90.08nS	P3	104.0nS	P4	104.1nS
P5	128.7nS	P6	137.2nS	P7	126.9nS
DEC0	61.19nS	DEC1	63.27nS	DEC2	57.84nS
DEC3	62.46nS	DEC4	66.98nS	DEC5	61.89nS

DEC6	57.48nS	DEC7	59.53nS	DEC8	51.72nS
DEC9	53.72nS	DEC10	57.84nS	DEC11	50.81nS
DEC12	52.19nS	DEC13	54.01nS	DEC14	56.83nS
DEC15	52.06nS	DEC16	58.29nS	DEC17	59.01nS
DEC18	57.90nS	DEC19	58.78nS	DEC20	56.63nS
DEC21	58.00nS	DEC22	54.08nS	DEC23	58.00nS
DEC24	64.04nS	DEC25	66.72nS	DEC26	60.36nS
DEC27	67.44nS	DEC28	67.13nS	DEC29	60.18nS
DEC30	64.25nS	DEC31	68.51nS	DEC32	69.23nS
DEC33	66.07nS	DEC34	75.04nS	DEC35	67.47nS
DEC36	67.42nS	DEC37	72.73nS	DEC38	67.44nS
DEC39	66.95nS	MOUT40	83.16nS	MOUT41	84.77nS
MOUT42	79.04nS	MOUT43	77.07nS	MOUT44	71.57nS
MOUT45	73.56nS	MOUT46	77.22nS	MOUT47	71.93nS
DEC0B	56.78nS	DEC1B	59.66nS	DEC2B	59.35nS
DEC3B	57.01nS	DEC4B	56.60nS	DEC5B	56.16nS
DEC6B	55.91nS	DEC7B	58.60nS	DEC8B	49.10nS
DEC9B	50.37nS	DEC10B	52.14nS	DEC11B	52.48nS
DEC12B	48.45nS	DEC13B	49.85nS	DEC14B	49.67nS
DEC15B	58.52nS	DEC16B	56.13nS	DEC17B	55.85nS
DEC18B	56.91nS	DEC19B	57.17nS	DEC20B	54.55nS
DEC21B	56.55nS	DEC22B	56.44nS	DEC23B	53.85nS
DEC24B	59.14nS	DEC25B	51.13nS	DEC26B	50.92nS
DEC27B	52.68nS	DEC28B	59.32nS	DEC29B	56.63nS
DEC30B	51.05nS	DEC31B	54.24nS	DEC32B	56.37nS
DEC33B	57.59nS	DEC34B	56.34nS	DEC35B	56.70nS
DEC36B	56.63nS	DEC37B	55.82nS	DEC38B	53.31nS
DEC39B	58.44nS	OUT40B	78.34nS	OUT41B	63.89nS
OUT42B	71.70nS	OUT43B	74.45nS	OUT44B	77.22nS
OUT45B	73.23nS	OUT46B	68.25nS	OUT47B	72.94nS

Tplhck params: Vcc = 5.00V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

Q0	28.56nS	Q1	33.07nS	Q2	30.97nS
Q3	33.05nS	Q0B	31.49nS	Q1B	34.08nS
Q2B	32.42nS	Q3B	30.37nS	TOUTA	27.88nS
QOUTA	15.32nS	TOUTB	26.64nS	QOUTB	15.74nS
MKTOUT	19.84nS	MKOUTB	19.76nS	MMOUT	65.50nS
COUT	65.16nS	P0	61.63nS	P1	79.25nS
P2	88.04nS	P3	101.0nS	P4	101.0nS
P5	124.6nS	P6	133.5nS	P7	123.1nS
DEC0	59.25nS	DEC1	61.45nS	DEC2	55.95nS
DEC3	60.05nS	DEC4	65.06nS	DEC5	60.02nS
DEC6	55.74nS	DEC7	57.77nS	DEC8	49.98nS
DEC9	51.64nS	DEC10	56.05nS	DEC11	49.70nS
DEC12	50.53nS	DEC13	52.35nS	DEC14	55.12nS
DEC15	50.37nS	DEC16	56.52nS	DEC17	57.40nS
DEC18	56.29nS	DEC19	57.14nS	DEC20	54.97nS
DEC21	56.31nS	DEC22	52.66nS	DEC23	56.34nS
DEC24	62.31nS	DEC25	64.93nS	DEC26	58.49nS
DEC27	65.55nS	DEC28	65.34nS	DEC29	58.52nS
DEC30	62.46nS	DEC31	66.59nS	DEC32	67.34nS
DEC33	64.23nS	DEC34	73.20nS	DEC35	65.63nS
DEC36	65.55nS	DEC37	70.81nS	DEC38	65.63nS
DEC39	65.00nS	MOUT40	80.70nS	MOUT41	82.10nS
MOUT42	76.96nS	MOUT43	74.84nS	MOUT44	69.21nS
MOUT45	71.28nS	MOUT46	75.04nS	MOUT47	69.65nS
DEC0B	55.04nS	DEC1B	57.46nS	DEC2B	57.46nS
DEC3B	54.99nS	DEC4B	54.68nS	DEC5B	54.39nS
DEC6B	56.94nS	DEC7B	56.76nS	DEC8B	47.57nS

DEC9B	48.74nS	DEC10B	50.58nS	DEC11B	50.81nS
DEC12B	47.05nS	DEC13B	48.32nS	DEC14B	48.12nS
DEC15B	56.83nS	DEC16B	56.39nS	DEC17B	54.68nS
DEC18B	54.97nS	DEC19B	55.12nS	DEC20B	52.99nS
DEC21B	54.91nS	DEC22B	54.84nS	DEC23B	52.42nS
DEC24B	57.30nS	DEC25B	49.49nS	DEC26B	49.34nS
DEC27B	51.05nS	DEC28B	57.59nS	DEC29B	54.89nS
DEC30B	49.41nS	DEC31B	52.58nS	DEC32B	54.60nS
DEC33B	56.34nS	DEC34B	54.68nS	DEC35B	54.91nS
DEC36B	54.99nS	DEC37B	54.08nS	DEC38B	51.64nS
DEC39B	56.63nS	OUT40B	76.20nS	OUT41B	62.15nS
OUT42B	69.28nS	OUT43B	72.06nS	OUT44B	75.04nS
OUT45B	70.89nS	OUT46B	66.09nS	OUT47B	70.45nS

Tplhck params: Vcc = 5.25V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	27.60nS	Q1	32.06nS	Q2	29.91nS
Q3	31.96nS	Q0B	30.53nS	Q1B	33.15nS
Q2B	31.18nS	Q3B	29.36nS	TOUTA	27.03nS
QOUTA	15.20nS	TOUTB	25.73nS	QOUTB	15.12nS
MKTOUT	19.17nS	MKOUTB	19.14nS	MMOUT	63.73nS
COUT	63.27nS	P0	60.10nS	P1	77.22nS
P2	85.81nS	P3	98.31nS	P4	98.18nS
P5	121.5nS	P6	130.2nS	P7	119.8nS
DEC0	57.69nS	DEC1	59.95nS	DEC2	54.50nS
DEC3	59.09nS	DEC4	63.34nS	DEC5	58.54nS
DEC6	54.32nS	DEC7	56.39nS	DEC8	48.48nS
DEC9	50.53nS	DEC10	54.60nS	DEC11	48.25nS
DEC12	48.97nS	DEC13	51.07nS	DEC14	53.69nS
DEC15	48.82nS	DEC16	55.07nS	DEC17	55.98nS
DEC18	54.97nS	DEC19	55.82nS	DEC20	53.64nS
DEC21	54.97nS	DEC22	51.41nS	DEC23	54.97nS
DEC24	60.80nS	DEC25	63.27nS	DEC26	57.07nS
DEC27	63.89nS	DEC28	63.81nS	DEC29	57.01nS
DEC30	61.01nS	DEC31	64.95nS	DEC32	65.65nS
DEC33	62.72nS	DEC34	71.51nS	DEC35	64.04nS
DEC36	64.10nS	DEC37	69.20nS	DEC38	64.12nS
DEC39	63.34nS	MOUT40	76.75nS	MOUT41	80.26nS
MOUT42	75.02nS	MOUT43	72.97nS	MOUT44	67.26nS
MOUT45	69.34nS	MOUT46	73.23nS	MOUT47	67.47nS
DEC0B	53.46nS	DEC1B	55.80nS	DEC2B	55.90nS
DEC3B	53.51nS	DEC4B	53.02nS	DEC5B	52.84nS
DEC6B	55.15nS	DEC7B	55.30nS	DEC8B	46.28nS
DEC9B	47.30nS	DEC10B	49.26nS	DEC11B	49.88nS
DEC12B	45.76nS	DEC13B	47.05nS	DEC14B	46.90nS
DEC15B	55.54nS	DEC16B	54.99nS	DEC17B	53.31nS
DEC18B	53.72nS	DEC19B	53.85nS	DEC20B	51.64nS
DEC21B	53.51nS	DEC22B	53.40nS	DEC23B	51.13nS
DEC24B	55.77nS	DEC25B	48.12nS	DEC26B	48.09nS
DEC27B	49.65nS	DEC28B	56.21nS	DEC29B	53.43nS
DEC30B	48.09nS	DEC31B	51.13nS	DEC32B	53.15nS
DEC33B	54.97nS	DEC34B	53.31nS	DEC35B	53.43nS
DEC36B	53.72nS	DEC37B	52.63nS	DEC38B	50.30nS
DEC39B	55.09nS	OUT40B	74.47nS	OUT41B	60.49nS
OUT42B	67.21nS	OUT43B	69.91nS	OUT44B	73.23nS
OUT45B	69.06nS	OUT46B	63.94nS	OUT47B	68.38nS

Tplhck params: Vcc = 5.5CV, Vih = 3.CCV, Vil = 0.CCV
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	26.79nS	Q1	31.26nS	Q2	29.10nS

Q3	30.97nS	QOB	29.73nS	Q1B	32.29nS
Q2B	30.32nS	Q3B	28.51nS	TOUTA	26.20nS
QOUTA	14.73nS	TOUTB	25.08nS	QOUTB	14.68nS
MKTOUT	18.68nS	MKOUTB	18.60nS	MMOUT	62.23nS
COUT	61.68nS	P0	58.72nS	P1	75.56nS
P2	83.86nS	P3	96.05nS	P4	95.90nS
P5	118.7nS	P6	126.9nS	P7	117.0nS
DEC0	56.39nS	DEC1	58.62nS	DEC2	53.31nS
DEC3	57.82nS	DEC4	61.87nS	DEC5	57.17nS
DEC6	52.94nS	DEC7	55.20nS	DEC8	47.26nS
DEC9	48.87nS	DEC10	53.38nS	DEC11	47.05nS
DEC12	48.01nS	DEC13	49.83nS	DEC14	52.48nS
DEC15	47.49nS	DEC16	53.82nS	DEC17	54.89nS
DEC18	53.77nS	DEC19	54.60nS	DEC20	52.48nS
DEC21	53.77nS	DEC22	50.30nS	DEC23	53.75nS
DEC24	59.61nS	DEC25	62.02nS	DEC26	55.85nS
DEC27	62.85nS	DEC28	62.46nS	DEC29	55.69nS
DEC30	59.74nS	DEC31	63.58nS	DEC32	64.25nS
DEC33	61.32nS	DEC34	70.19nS	DEC35	62.77nS
DEC36	62.93nS	DEC37	67.86nS	DEC38	62.85nS
DEC39	62.02nS	MOUT40	76.90nS	MOUT41	78.34nS
MOUT42	73.36nS	MOUT43	71.44nS	MOUT44	65.76nS
MOUT45	67.94nS	MOUT46	71.67nS	MOUT47	65.65nS
DEC0B	52.22nS	DEC1B	54.65nS	DEC2B	54.58nS
DEC3B	52.19nS	DEC4B	51.64nS	DEC5B	51.52nS
DEC6B	53.67nS	DEC7B	53.93nS	DEC8B	45.24nS
DEC9B	46.25nS	DEC10B	48.04nS	DEC11B	48.32nS
DEC12B	44.72nS	DEC13B	45.94nS	DEC14B	45.81nS
DEC15B	54.32nS	DEC16B	53.75nS	DEC17B	51.77nS
DEC18B	52.19nS	DEC19B	52.50nS	DEC20B	50.53nS
DEC21B	52.29nS	DEC22B	52.22nS	DEC23B	50.04nS
DEC24B	54.47nS	DEC25B	46.92nS	DEC26B	46.90nS
DEC27B	48.43nS	DEC28B	54.97nS	DEC29B	52.06nS
DEC30B	46.87nS	DEC31B	49.91nS	DEC32B	51.98nS
DEC33B	53.72nS	DEC34B	51.77nS	DEC35B	52.24nS
DEC36B	52.48nS	DEC37B	51.52nS	DEC38B	49.18nS
DEC39B	53.85nS	OUT40B	72.92nS	OUT41B	59.12nS
OUT42B	65.57nS	OUT43B	68.25nS	OUT44B	71.70nS
OUT45B	67.42nS	OUT46B	62.77nS	OUT47B	66.61nS

Tphlck params: Vcc = 4.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	37.97nS	Q1	41.01nS	Q2	38.83nS
Q3	40.85nS	Q0B	40.23nS	Q1B	42.80nS
Q2B	42.85nS	Q3B	38.39nS	TOUTA	36.83nS
QOUTA	24.85nS	TOUTB	35.85nS	QOUTB	24.77nS
MKTOUT	28.27nS	MKOUTB	28.12nS	MMOUT	53.90nS
COUT	74.16nS	P0	67.13nS	P1	84.98nS
P2	97.74nS	P3	114.8nS	P4	114.7nS
P5	136.9nS	P6	141.0nS	P7	120.3nS
DEC0	69.10nS	DEC1	73.36nS	DEC2	70.66nS
DEC3	69.65nS	DEC4	74.86nS	DEC5	70.53nS
DEC6	68.74nS	DEC7	68.87nS	DEC8	57.64nS
DEC9	63.68nS	DEC10	66.12nS	DEC11	59.19nS
DEC12	60.49nS	DEC13	64.77nS	DEC14	64.15nS
DEC15	60.52nS	DEC16	67.34nS	DEC17	65.29nS
DEC18	67.05nS	DEC19	64.30nS	DEC20	64.10nS
DEC21	65.42nS	DEC22	65.39nS	DEC23	64.87nS
DEC24	69.49nS	DEC25	78.00nS	DEC26	68.25nS
DEC27	77.07nS	DEC28	76.86nS	DEC29	71.41nS
DEC30	73.15nS	DEC31	78.41nS	DEC32	76.16nS
DEC33	77.53nS	DEC34	83.06nS	DEC35	76.05nS
DEC36	76.75nS	DEC37	80.85nS	DEC38	77.61nS
DEC39	74.99nS	MOUT40	87.75nS	MOUT41	92.06nS
MOUT42	85.94nS	MOUT43	81.53nS	MOUT44	78.41nS
MOUT45	78.75nS	MOUT46	85.39nS	MOUT47	76.96nS
DEC0B	68.12nS	DEC1B	68.25nS	DEC2B	65.47nS
DEC3B	65.37nS	DEC4B	64.80nS	DEC5B	64.87nS
DEC6B	68.25nS	DEC7B	66.59nS	DEC8B	54.26nS
DEC9B	59.66nS	DEC10B	60.93nS	DEC11B	62.70nS
DEC12B	57.25nS	DEC13B	60.49nS	DEC14B	58.49nS
DEC15B	70.43nS	DEC16B	65.42nS	DEC17B	65.50nS
DEC16B	64.96nS	DEC19B	65.50nS	DEC2CB	61.61nS
DEC21B	64.85nS	DEC22B	66.74nS	DEC23B	63.24nS
DEC24B	67.05nS	DEC25B	59.66nS	DEC26B	61.40nS
DEC27B	60.08nS	DEC28B	63.66nS	DEC29B	66.98nS
DEC30B	60.46nS	DEC31B	58.91nS	DEC32B	64.41nS
DEC33B	65.89nS	DEC34B	67.49nS	DEC35B	66.43nS
DEC36B	64.85nS	DEC37B	65.73nS	DEC38B	63.19nS
DEC39B	68.17nS	OUT40B	79.58nS	OUT41B	72.53nS
OUT42B	75.74nS	OUT43B	77.38nS	OUT44B	78.00nS
OUT45B	77.48nS	OUT46B	77.09nS	OUT47B	78.21nS

Tphlck params: Vcc = 4.75V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	36.63nS	Q1	39.95nS	Q2	37.84nS
Q3	39.53nS	Q0B	38.96nS	Q1B	41.63nS
Q2B	41.79nS	Q3B	37.22nS	TOUTA	35.90nS
QOUTA	24.17nS	TOUTB	34.84nS	QOUTB	24.12nS
MKTOUT	27.57nS	MKOUTB	27.37nS	MMOUT	52.29nS
COUT	72.06nS	P0	65.06nS	P1	82.59nS
P2	94.91nS	P3	111.3nS	P4	111.1nS
P5	133.0nS	P6	136.4nS	P7	116.4nS
DEC0	67.26nS	DEC1	71.28nS	DEC2	68.64nS
DEC3	67.78nS	DEC4	72.86nS	DEC5	68.51nS

DEC6	66.79nS	DEC7	67.00nS	DEC8	56.03nS
DEC9	61.84nS	DEC10	64.28nS	DEC11	56.88nS
DEC12	58.70nS	DEC13	62.88nS	DEC14	62.44nS
DEC15	58.80nS	DEC16	65.70nS	DEC17	63.58nS
DEC18	65.47nS	DEC19	63.19nS	DEC20	62.41nS
DEC21	63.81nS	DEC22	63.81nS	DEC23	63.32nS
DEC24	67.49nS	DEC25	76.05nS	DEC26	66.59nS
DEC27	75.17nS	DEC28	74.81nS	DEC29	69.34nS
DEC30	71.20nS	DEC31	76.52nS	DEC32	74.32nS
DEC33	75.64nS	DEC34	80.85nS	DEC35	73.77nS
DEC36	74.89nS	DEC37	78.70nS	DEC38	75.82nS
DEC39	73.15nS	MOUT40	85.39nS	MOUT41	89.72nS
MOUT42	83.73nS	MOUT43	79.04nS	MOUT44	76.26nS
MOUT45	76.55nS	MOUT46	82.90nS	MOUT47	74.60nS
DEC0B	66.12nS	DEC1B	66.20nS	DEC2B	63.71nS
DEC3B	63.42nS	DEC4B	62.95nS	DEC5B	62.85nS
DEC6B	66.28nS	DEC7B	64.69nS	DEC8B	52.60nS
DEC9B	58.03nS	DEC10B	59.22nS	DEC11B	61.04nS
DEC12B	55.77nS	DEC13B	58.70nS	DEC14B	57.14nS
DEC15B	66.40nS	DEC16B	63.81nS	DEC17B	63.81nS
DEC18B	63.34nS	DEC19B	63.81nS	DEC20B	59.87nS
DEC21B	63.01nS	DEC22B	65.03nS	DEC23B	61.55nS
DEC24B	65.19nS	DEC25B	58.00nS	DEC26B	59.69nS
DEC27B	58.34nS	DEC28B	65.72nS	DEC29B	65.06nS
DEC30B	58.60nS	DEC31B	57.25nS	DEC32B	62.70nS
DEC33B	64.17nS	DEC34B	65.70nS	DEC35B	65.21nS
DEC36B	63.16nS	DEC37B	63.97nS	DEC38B	61.53nS
DEC39B	66.40nS	OUT40B	77.38nS	OUT41B	70.58nS
OUT42B	73.77nS	OUT43B	75.15nS	OUT44B	76.05nS
OUT45B	75.43nS	OUT46B	74.89nS	OUT47B	75.72nS

Tphlck params: Vcc = 5.00V, Vih = 3.00V, Vil = 0.00V
Limits: 1.00CnS minimum, 200.0nS maximum.

Q0	35.93nS	Q1	39.04nS	Q2	37.07nS
Q3	38.49nS	Q0B	38.05nS	Q1B	40.70nS
Q2B	40.93nS	Q3B	36.21nS	TOUTA	34.97nS
QOUTA	23.63nS	TOUTB	33.93nS	QOUTB	23.50nS
MKTOUT	27.03nS	MKOUTB	26.72nS	MMOUT	51.00nS
COUT	70.27nS	P0	63.27nS	P1	80.52nS
P2	92.53nS	P3	108.2nS	P4	108.2nS
P5	129.2nS	P6	132.7nS	P7	113.1nS
DEC0	65.65nS	DEC1	69.60nS	DEC2	66.98nS
DEC3	66.12nS	DEC4	71.18nS	DEC5	66.82nS
DEC6	65.16nS	DEC7	65.32nS	DEC8	54.50nS
DEC9	60.36nS	DEC10	62.72nS	DEC11	56.08nS
DEC12	57.17nS	DEC13	61.29nS	DEC14	60.80nS
DEC15	57.25nS	DEC16	64.25nS	DEC17	62.25nS
DEC18	64.10nS	DEC19	61.63nS	DEC20	60.93nS
DEC21	62.36nS	DEC22	62.41nS	DEC23	61.87nS
DEC24	65.81nS	DEC25	74.37nS	DEC26	64.93nS
DEC27	73.46nS	DEC28	73.10nS	DEC29	67.78nS
DEC30	69.36nS	DEC31	74.84nS	DEC32	72.60nS
DEC33	73.95nS	DEC34	79.04nS	DEC35	72.14nS
DEC36	73.15nS	DEC37	76.94nS	DEC38	74.19nS
DEC39	71.51nS	MOUT40	83.47nS	MOUT41	87.34nS
MOUT42	81.55nS	MOUT43	77.09nS	MOUT44	74.58nS
MOUT45	74.86nS	MOUT46	80.70nS	MOUT47	72.53nS
DEC0B	64.56nS	DEC1B	64.54nS	DEC2B	62.07nS
DEC3B	61.94nS	DEC4B	61.37nS	DEC5B	61.14nS
DEC6B	64.64nS	DEC7B	63.01nS	DEC8B	51.20nS

DEC9B	56.63nS	DEC10B	57.69nS	DEC11B	59.40nS
DEC12B	54.45nS	DEC13B	57.17nS	DEC14B	55.61nS
DEC15B	66.87nS	DEC16B	62.33nS	DEC17B	62.33nS
DEC18B	61.92nS	DEC19B	62.25nS	DEC20B	58.49nS
DEC21B	61.61nS	DEC22B	63.55nS	DEC23B	60.15nS
DEC24B	63.55nS	DEC25B	56.52nS	DEC26B	58.23nS
DEC27B	56.99nS	DEC28B	65.16nS	DEC29B	63.60nS
DEC30B	57.09nS	DEC31B	55.90nS	DEC32B	61.22nS
DEC33B	62.62nS	DEC34B	64.25nS	DEC35B	63.11nS
DEC36B	61.63nS	DEC37B	62.25nS	DEC38B	59.95nS
DEC39B	64.93nS	OUT40B	75.43nS	OUT41B	68.79nS
OUT42B	71.57nS	OUT43B	73.38nS	OUT44B	74.29nS
OUT45B	73.64nS	OUT46B	72.94nS	OUT47B	73.77nS

Tphlck params: Vcc = 5.25V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

Q0	35.07nS	Q1	38.29nS	Q2	36.37nS
Q3	37.56nS	Q3B	37.14nS	Q1B	39.92nS
Q2B	40.10nS	TOUTB	35.30nS	TOUTA	34.16nS
QOUTA	23.09nS	MKOUTB	33.25nS	QOUTB	23.01nS
MKTOUT	26.41nS	P0	26.25nS	MMOUT	49.75nS
COUT	68.56nS	P3	61.61nS	P1	78.62nS
P2	90.37nS	P6	105.6nS	P4	105.7nS
P5	126.0nS	DEC1	129.2nS	P7	110.3nS
DEC0	64.25nS	DEC4	67.96nS	DEC2	65.60nS
DEC3	64.77nS	DEC7	69.49nS	DEC5	65.34nS
DEC6	63.78nS	DEC10	63.81nS	DEC8	53.20nS
DEC9	58.83nS	DEC13	61.37nS	DEC11	54.39nS
DEC12	55.80nS	DEC16	59.76nS	DEC14	59.45nS
DEC15	56.00nS	DEC19	63.03nS	DEC17	60.96nS
DEC18	62.80nS	DEC22	60.46nS	DEC20	59.58nS
DEC21	61.16nS	DEC25	61.27nS	DEC23	60.70nS
DEC24	64.36nS	DEC28	72.81nS	DEC26	63.81nS
DEC27	71.98nS	DEC31	71.57nS	DEC29	66.28nS
DEC30	67.88nS	DEC34	73.38nS	DEC32	71.18nS
DEC33	72.45nS	DEC37	77.38nS	DEC35	70.74nS
DEC36	71.80nS	MOUT40	75.38nS	DEC38	72.68nS
DEC39	69.96nS	MOUT43	81.53nS	MOUT41	85.42nS
MOUT42	79.70nS	MOUT46	75.46nS	MOUT44	72.92nS
MOUT45	73.23nS	DEC1B	78.70nS	MOUT47	70.74nS
DEC0B	63.19nS	DEC4B	63.16nS	DEC2B	60.62nS
DEC3B	60.49nS	DEC7B	59.95nS	DEC5B	59.40nS
DEC6B	62.98nS	DEC10B	61.53nS	DEC8B	49.91nS
DEC9B	55.38nS	DEC13B	56.44nS	DEC11B	57.74nS
DEC12B	53.23nS	DEC16B	55.85nS	DEC14B	54.65nS
DEC15B	65.47nS	DEC19B	61.04nS	DEC17B	61.04nS
DEC18B	60.65nS	DEC22B	61.32nS	DEC20B	57.25nS
DEC21B	60.33nS	DEC25B	62.33nS	DEC23B	58.83nS
DEC24B	62.15nS	DEC28B	55.30nS	DEC26B	56.94nS
DEC27B	55.74nS	DEC31B	63.73nS	DEC29B	62.18nS
DEC30B	55.85nS	DEC34B	54.65nS	DEC32B	59.71nS
DEC33B	61.14nS	DEC37B	62.93nS	DEC35B	62.31nS
DEC36B	60.33nS	OUT40B	60.88nS	DEC38B	58.44nS
DEC39B	63.58nS	OUT43B	73.77nS	OUT41B	67.21nS
OUT42B	69.91nS	OUT46B	71.67nS	OUT44B	72.81nS
OUT45B	72.11nS		71.26nS	OUT47B	72.11nS

Tphlck params: Vcc = 5.50V, Vih = 3.00V, Vil = 0.00V
Limits: 1.000nS minimum, 200.0nS maximum.

Q0	34.34nS	Q1	37.61nS	Q2	35.69nS

Q3	36.86nS	QOB	36.44nS	Q1B	39.22nS
Q2B	39.25nS	Q3B	34.60nS	TOUTA	33.51nS
QOUTA	22.64nS	TOUTB	32.53nS	QOUTB	22.57nS
MKTOUT	25.94nS	MKOUTB	25.73nS	MMOUT	48.77nS
COUT	67.11nS	P0	60.31nS	P1	77.01nS
P2	88.38nS	P3	103.3nS	P4	103.6nS
P5	123.0nS	P6	126.2nS	P7	107.8nS
DEC0	63.03nS	DEC1	66.59nS	DEC2	64.25nS
DEC3	63.50nS	DEC4	63.12nS	DEC5	64.10nS
DEC6	62.44nS	DEC7	62.57nS	DEC8	52.03nS
DEC9	57.46nS	DEC10	60.10nS	DEC11	52.94nS
DEC12	54.68nS	DEC13	58.47nS	DEC14	58.29nS
DEC15	54.97nS	DEC16	61.92nS	DEC17	59.69nS
DEC18	61.79nS	DEC19	59.22nS	DEC20	58.49nS
DEC21	59.95nS	DEC22	60.23nS	DEC23	59.61nS
DEC24	63.01nS	DEC25	71.44nS	DEC26	62.44nS
DEC27	70.66nS	DEC28	70.22nS	DEC29	65.03nS
DEC30	66.43nS	DEC31	71.98nS	DEC32	69.73nS
DEC33	71.15nS	DEC34	75.85nS	DEC35	69.34nS
DEC36	70.35nS	DEC37	73.77nS	DEC38	71.44nS
DEC39	68.64nS	MOUT40	79.87nS	MOUT41	83.81nS
MOUT42	78.08nS	MOUT43	74.06nS	MOUT44	71.49nS
MOUT45	71.70nS	MOUT46	76.96nS	MOUT47	67.70nS
DEC0B	61.84nS	DEC1B	61.87nS	DEC2B	59.25nS
DEC3B	58.86nS	DEC4B	58.67nS	DEC5B	58.00nS
DEC6B	61.61nS	DEC7B	60.23nS	DEC8B	48.79nS
DEC9B	54.26nS	DEC10B	55.35nS	DEC11B	56.47nS
DEC12B	52.19nS	DEC13B	54.89nS	DEC14B	53.59nS
DEC15B	64.12nS	DEC16B	59.79nS	DEC17B	59.79nS
DEC18B	59.48nS	DEC19B	59.95nS	DEC20B	56.31nS
DEC21B	59.12nS	DEC22B	61.14nS	DEC23B	57.66nS
DEC24B	60.93nS	DEC25B	54.16nS	DEC26B	55.72nS
DEC27B	54.65nS	DEC28B	62.46nS	DEC29B	60.91nS
DEC30B	54.73nS	DEC31B	53.51nS	DEC32B	58.47nS
DEC33B	59.38nS	DEC34B	61.76nS	DEC35B	61.04nS
DEC36B	59.01nS	DEC37B	59.53nS	DEC38B	57.25nS
DEC39B	62.36nS	OUT40B	72.11nS	OUT41B	65.89nS
OUT42B	68.27nS	OUT43B	70.06nS	OUT44B	71.36nS
OUT45B	70.66nS	OUT46B	67.05nS	OUT47B	70.45nS

Device PASSED all tests.

SECTION 3.6
Life Test Results (500 hr)

ACTEL 1280 FPGA LIFE TEST RESULTS

240 HOURS-TEMP=25°C

TEST	UNIT1-2-CTL	UNIT3	UNIT4	UNIT5	UNIT6	UNIT7	UNIT8	UNIT9	UNIT10	UNIT11	UNIT12
FUNC	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VOH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VOL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
ISB	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IIH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IOZL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IOZH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VIH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPZL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPZH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPLHCK	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPHLCK	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

ACTEL 1280 FPGA LIFE TEST RESULTS

500 HOURS-TEMP=25°C

TEST	UNIT1-2-CTL	UNIT3	UNIT4	UNIT5	UNIT6	UNIT7	UNIT8	UNIT9	UNIT10	UNIT11	UNIT12
FUNC	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VOH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VOL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
ISB	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IIH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IOZL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IOZH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VIH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPZL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPZH	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPLHCK	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
TPHLCK	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

9-Jun-92

ACTEL 1280 FPGA LIFE TESTS PERFORMED

TEST	CONDITIONS	# PINS
FUNC	VCC = 4.50V, VIH = 3.00V,VIL = 0.00V	
	VCC = 4.75V,VIH = 3.00V,VIL = 0.00V	
	VCC = 5.00V,VIH = 3.00V,VIL = 0.00V	
	VCC = 5.25V,VIH = 3.00V,VIL = 0.00V	
	VCC = 5.50V,VIH = 3.00V,VIL = 0.00V	
VOH	VCC = 4.50V,VIH = 3.00V,VIL = 0.00V,Io = -4.00ma,LIMIT = 3.70V MIN,5.50V MAX	120
	VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,Io = -4.00ma,LIMIT = 3.70V MIN,5.50V MAX	120
	VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,Io = -4.00ma, LIMIT = 3.70V MIN,5.50V MAX	120
	VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,Io = -4.00ma,LIMIT = 3.70V MIN,5.50V MAX	120
	VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,Io = -4.00ma,LIMIT = 3.70V MIN,5.50V MAX	120
VOL	VCC = 4.40V,VIH = 3.00V,VIL = 0.00V,Io = 6.00ma,LIMIT = 0.00V MIN,0.400V MAX	120
	VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,Io = 6.00ma,LIMIT = 0.00V MIN,0.400V MAX	120
	VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,Io = 6.00ma,LIMIT = 0.00V MIN,0.400V MAX	120
	VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,Io = 6.00ma,LIMIT = 0.00V MIN,0.400V MAX	120
	VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,Io = 6.00ma,LIMIT = 0.00V MIN,0.400V MAX	120
Isb	VCC = 4.50V,INS = 4.50V,OUTS = OPEN,LIMIT = 123.3ua MIN,25ma MAX	1
	VCC = 4.75V,INS = 4.75V,OUTS = OPEN,LIMIT = 133.3ua MIN,25ma MAX	1
	VCC = 5.00V,INS = 5.00V,OUTS = OPEN,LIMIT = 180.0ua MIN,25ma MAX	1
	VCC = 5.25V,INS = 5.25V,OUTS = OPEN,LIMIT = 210.0ua MIN,25ma MAX	1
	VCC = 5.50V,INS = 5.50V,OUTS = OPEN,LIMIT = 240.0ua MIN,25ma MAX	1
Iil	VCC = 4.50V,VIN = 0.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 4.75V,VIN = 0.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.00V,VIN = 0.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.25V,VIN = 0.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.50V,VIN = 0.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
Iih	VCC = 4.50V,VIN = 4.50V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 4.75V,VIN = 4.75V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.00V,VIN = 5.00V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.25V,VIN = 5.25V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
	VCC = 5.50V,VIN = 5.50V,LIMIT = -10.00ua MIN,+ 10.00ua MAX	23
Iozl	VCC = 4.50V,VIN = 0.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 4.75V,VIN = 0.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.00V,VIN = 0.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.25V,VIN = 0.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.50V,VIN = 0.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
Iozh	VCC = 4.50V,VIN = 4.50V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 4.75V,VIN = 4.75V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.00V,VIN = 5.00V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.25V,VIN = 5.25V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120
	VCC = 5.50V,VIN = 5.50V,LIMIT = -10.00ua, MIN,+ 10.00ua MAX	120

	Vih	VCC = 4.50V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 4.75V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.00V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.25V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.00V,LIMIT = 800.0mv MIN,2.00V MAX							23
	Vil	VCC = 4.50V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 4.75V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.00V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.25V,LIMIT = 800.0mv MIN,2.00V MAX							23
		VCC = 5.00V,LIMIT = 800.0mv MIN,2.00V MAX							23
	Tpzl	VCC = 4.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
	Tpzh	VCC = 4.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
		VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							112
	Tplhck	VCC = 4.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
	Tphlck	VCC = 4.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 4.75V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.00V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.25V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120
		VCC = 5.50V,VIH = 3.00V,VIL = 0.00V,LIMIT = 1.00ns MIN,200.0ns MAX							120

SECTION 3.7
Radiation Data Total Dose

1.0 Purpose

The purpose of this test is to characterize the Actel 1280, 1.2um CMOS FPGA, for space application total dose environments.

2.0 Background

Previous total dose testing of the Actel 1020, 2.0um CMOS FPGA performed by Hughes Aircraft Company (HAC) found a significant increase in the minimum Vdd during post rad ambient (25 deg C) annealing testing. In addition, a two to three times increase in Idd was observed. The Actel 1020 tests concluded that the 1020 device was acceptable to 100K rad. Since the Actel 1280, 1.2um component is based on the same process similar results were expect. During the Actel 1280 testing, a focus was placed on the increases in the Vdd and Idd.

3.0 Test Procedure

The test procedure used to evaluate the Actel 1280 device is identical to the procedure used for the 1020 device. A copy of the test procedure is provided in Appendix A. A summary of the procedure is described below:

Test A: Tri-state output buffer characterization.
Measure the following parameters of the tri-state output buffer:
Voh, Vol, Ios, Leakage, Tr, Tf, Tplh, Tphl, Tphz, Tpzh, Tplz, Tpzl
Four outputs per device are tested.

Test B: Standard input/output buffer characterization and combinatory logic delay test.
Measure the following parameters of the standard output buffer:
Voh, Vol, Ios, Vih, Vil, Iih, Iil, Tr, Tf, Tphl, Tplh
Four output/input per devices are tested.

Measure the delay through the following logic elements:
3 input AND, 4 input AND, 3 input OR, 4 input OR
50 gates of each type are changed together in series.
One chain of each gate type per device are tested.

Test C: Flip-Flop characterization.
Measure the following parameters of the D-type flop-flop:
Tsu, Thd, Tpd, minimum clock pulse width, clock skew
Four flip-flops are tested.
The clock skew measures the maximum clock skew across the entire die.

Test D: Speed and minimum Vdd characterization.
Measure the maximum operating frequency of a 12 bit binary counter.
Measure the minimum Vdd that the 12 bit binary counter will operate.
One counter per device is tested.
The counter fails the tests when it fails the functional count vectors.

Test E: Static Idd and dynamic Idd measurement.
Measure the static Idd.
Measure the dynamic Idd at 5Mhz, 2Mhz, and 1Mhz.

4.0 Test Samples

A total of 26 sample parts are used from two diffusion lots (13 from each lot). The parts were provided by Actel. Both lots are from the Matsushita's 1.2um production process. All parts are programmed at HAC. Twenty-four parts are for testing and two are for control.

5.0 Test Flow

Test samples shall be divided into four groups of six (three devices from each diffusion lot). Each group shall be exposed at a single total dose level then annealed in accordance with Table 1. Electrical tests shall be performed pre-rad, post-rad, and following each annealing period. Bias voltage shall be maintained during exposure, anneal, and transportation periods. Unbiased periods shall not exceed one minute at any one time.

Group Number	Quantity	Total Dose (K rad)	Anneal Procedure (Cumulative hours)
1	6	20	1 hour at 25 deg C 3 hours at 25 deg C 24 hours at 100 deg C 48 hours at 100 deg C 72 hours at 100 deg C 168 hours at 100 deg C
2	6	70	Same as above
3 *	6	100	Same as above
4 *	6	200	Same as above

Table 1 - Total Dose Levels and Anneal Procedure

* Note: These levels were not performed due to the 70K rad test results.

6.0 Bias Conditions

All devices are biased during irradiation, anneal, and transportation. This circuit holds the reset low to ensure that all parts are held in a fixed known state. Four outputs are held high while in the high Z state. The remaining outputs are left open with some driven low and some driven high.

Two bias boards are used. The exposure bias board holds two test samples, the anneal bias board holds six devices. Both bias boards use zero insertion force sockets.

7.0 Radiation Source

The two radiation sources used are the Hughes Gammacell 220, Cobalt 60 irradiators with dose rates of approximately 83.37 rad (Si)/sec and 123.59 rad (Si)/sec. These cells have a MIL-STD-883, Method 1019 compliant Pb-Al scatter cutter and temperature controller installed. Parts are irradiated two at a time, maintaining dose uniformity to within ten percent.

8.0 Test Result Summary

Group 2 (70 K rad) test was performed first. The cell is rated at 123.57 rad/sec. The total dose time is 9.48 minutes. A total of four parts (S/N 2, 3, 5, and 6) were irradiated to 70K rad. S/N 2 and 5 were irradiated first then tested, then S/N 3 and 6 were irradiated, then tested. The Idd current and temperature was monitored while the parts were irradiated. When the exposure started a rapid increase in Idd current was noticed. Within 90 seconds of the start of the exposure the Idd value reached 60ma per device. This was approximately a 350 times increase in the pre-rad Idd value. The power supply current limit was increased to 300ma (to yield 150ma per device) and within 140 seconds the Idd current reached 150ma per device. At this point the current limit of the power supply was not increased because of the risk of thermally damaging the devices. The power supplies current limited at 300ma (total for both devices) and the Vdd voltage dropped to 2.4 volts during the

remainder of the exposure. Once the exposure stopped, a rapid and steady decrease in Idd current was noticed. The devices were removed from the chamber and placed in the bias board for transportation to the test area. The total time that the devices were unbiased was less than one minute. Table 2 summarizes the Idd measurements for the "0 hour", "1 hour", and "3 hour" tests.

Static Idd (ma)				
Hour	S/N 2	S/N 5	S/N 3	S/N 6
"0 hr" (25 deg C)	23.9 actual time 46 min	no data available	79.0 actual time 21 min	25.3 actual time 23 min
"1 hr" (25 deg C)	22.9 actual time 1 hr 6 min	16.8 actual time 1 hr 29 min	60.4 actual time 1 hr 2 min	20.7 actual time 1 hr 3 min
"3 hr" (25 deg C)	18.5 actual time 3 hr 22 min	14.9 actual time 3 hr 24 min	52.3 actual time 2 hr 0 min	18.6 actual time 2 hr 2 min

Table 2 - Static Idd Current - 70K rad - Ambient Anneal

In addition to the Idd measurements a complete set of tests corresponding the test procedure described in Appendix A was collected.

During device testing difficulty was encountered in powering-up the devices. The static Idd current decreased to a reasonable level quickly post-rad but the power-up (inrush) Idd current was very high. While testing the devices post-rad the current limit level of the tester power supply had to be set as high as 300ma to guarantee that the parts would power up to 5.0 volts. This is the reason that no data was available on S/N 5 "0 hr". The tester was set at it's maximum current limit value of 450ma and the device still would not power-up. Once the devices were at 5.0 volts the Idd current remained at it's static value.

During the post-rad testing a minimum Vdd test was performed. As described in the test procedure in Appendix A, a 12 bit binary counter was programmed in each device and clocked at 1 Mhz. The Vdd voltage was continuously decreased until the counter fails to count "correctly" (note, "correctly" means a simple functional check of the binary count sequence). This test was used to help assess threshold shifts due to radiation. The minimum Vdd observed pre-rad was 2.11 volts. This value was very consistent among all devices. Table 3 lists the minimum Vdd value during the ambient annealing period.

Minimum Vdd (volts)				
Hour	S/N 2	S/N 5	S/N 3	S/N 6
"0 hr" (25 deg C)	2.54 actual time 46 min	no data available	4.41 actual time 21 min	2.63 actual time 23 min
"1 hr" (25 deg C)	2.56 actual time 1 hr 6 min	2.79 actual time 1 hr 29 min	3.70 actual time 1 hr 2 min	2.64 actual time 1 hr 3 min
"3 hr" (25 deg C)	2.61 actual time 3 hr 22 min	2.84 actual time 3 hr 24 min	3.35 actual time 2 hr 0 min	2.66 actual time 2 hr 2 min

Table 3 - Minimum Vdd - 70K rad - Ambient Anneal

In general the minimum Vdd value increased post-rad during the ambient annealing period from the "0 hr" to the "3 hour" tests except for S/N 3.

Once the ambient annealing period was complete the high temperature annealing began. During high annealing, each devices was tested at 24, 48, 72, and 168 hours. The devices were biased and annealed at 125 deg C. The complete test procedure was performed on each device during each test time. Close attention was focused on the Idd current and the minimum Vdd value. Table 4 lists the Idd measurements during temperature annealing.

Static Idd (ma)				
Hour	S/N 2	S/N 5	S/N 3	S/N 6
24 hr (125 deg C)	80.6	94.1	111.0	92.0
48 hr (125 deg C)	62.8	70.6	86.6	65.7
72 hr (125 deg C)	54.9	57.1	73.9	46.2
168 hr (125 deg C)	20.1	18.5	33.6	14.4

Table 4 - Static Idd Current - 70K rad - Temperature Anneal

As shown in the Table 4, an large increase in Idd current occurred after the first 24 hours of temperature annealing for all devices and within 7 days fell off to a fairly low level.

The minimum Vdd displayed a continuous upward shift during the annealing period as shown in Table 5.

Minimum Vdd (volts)				
Hour	S/N 2	S/N 5	S/N 3	S/N 6
24 hr (125 deg C)	2.88	2.99	2.81	2.81
48 hr (125 deg C)	4.11	4.11	4.00	4.00
72 hr (125 deg C)	4.11	4.11	4.00	4.11
168 hr (125 deg C)	4.11	4.11	4.11	4.11

Table 5 - Minimum Vdd - 70K rad - Temperature Anneal

The minimum Vdd value clamped at approximately 4.11 volts for all devices. This is an 2 volt increase over the pre-rad value.

Based on the performance of the four devices at 70K rad, a lower value total dose test of 20K rad was performed next. In addition to a lower total dose value a different dose rate chamber was used. The chamber is rated at 83 rad/sec. A different dose rate chamber was selected in order to see if the dose rate would significantly affect the rate of Idd increase during the exposure period. Four devices (S/N 7, 8, 9, and 10) were tested pre-rad then irradiated biased to 20K rad. Like the 70K rad test, immediately after the exposure started a rapid increase in Idd current was observed. Within 180 seconds of the start of the exposure the Idd current reached 150ma per device. The power supply current limit was increased to 500ma (250ma per device) to prevent a current limit voltage drop.

During the exposure of S/N 7 and 8, at about 20 seconds before the end of the exposure period (the Idd current was now at approximately 200ma per device) a sudden jump in Idd current forced the power supply into current limit at 500ma (total for both devices) and the Vdd voltage to drop to 2.4 volts. The devices stayed in this high current mode for the remainder of the exposure period. It is unknown what caused the sudden (instantaneous) increase in Idd. Devices S/N 9 and 10 did not exhibit this problem. After the exposure was complete the devices were transported biased to the test area for the "0 hour", "1 hour", and "3 hour" tests. Same as for the 70K rad devices, a high inrush current was required in order to power-up the devices. In the 20K rad cases ALL devices would not power-up even with the tester power supply set to it's maximum value of 450 ma. Even after 3 hours of ambient annealing the devices would not power-up. At this point the devices were place in the oven to start temperature annealing. After 24 hours of temperature annealing the devices were tested, all devices powered-up correctly. Table 6 summarizes the Idd measurements during the post-rad temperature annealing period.

Static Idd (ma)				
Hour	S/N 7	S/N 8	S/N 9	S/N 10
24 hr (125 deg C)	2.21	.673	.750	.743
48 hr (125 deg C)	121.5	119.5	151.5	144.5
72 hr (125 deg C)	89.6	84.1	102.3	100.8
168 hr (125 deg C)	26.6	22.9	33.4	30.2

Table 6 - Static Idd Current - 20K rad - Temperature Anneal

Like in the 70K rad case, the Idd current increased during the initial annealing period and decreased to a fairly low level at the end of the 7 day period.

The minimum Vdd tests did not detect any real change in the Vdd value at 20K rad during the annealing period. Table 7 is a summary of the minimum Vdd test results.

Minimum Vdd (volts)				
Hour	S/N 7	S/N 8	S/N 9	S/N 10
24 hr (125 deg C)	1.2	2.00	2.00	2.00
48 hr (125 deg C)	2.00	2.05	2.25	2.00
72 hr (125 deg C)	2.00	2.00	2.00	2.00
168 hr (125 deg C)	2.00	2.00	2.00	2.00

Table 7 - Minimum Vdd - 20K rad - Temperature Anneal

The above documentation only discussed the two key parameters, Idd and minimum Vdd. The actually test performed measured a wide variety of parameters as described in Appendix A. Table 8 list some of the other parameters measured and the variation over the pre-rad value after the 7 day annealing period. Table 8 is data for the 70K rad case. 20K rad test data was also taken with similar results.

Test Name	Pre-Rad Value	Post-Anneal Value 70K Rad	Comments
tri-state buffer propagation delay Tphl	S/N 2 = 18.05 ns S/N 5 = 19.00ns	S/N 2 =18.20ns S/N 5 = 16.00ns	low-to-high measurement
tri-state buffer output voltage high Voh	S/N 2 = 4.81v S/N 5 = 4.79v	S/N 2 = 4.80v S/N 5 =4.79v	Ioh = 3.2ma
tri-state buffer output voltage low Vol	S/N 2 = .075v S/N 5 = .082v	S/N 2 = .080v S/N 5 = .085v	Iol = 4.0ma
tri-state buffer output current leakage Iozh	S/N 2 = 4.15na S/N 5 = 4.20na	S/N 2 = 6.17na S/N 5 = 5.04na	tri-state buffer in high-Z state with output tied to 5v.
4 input AND gate propagation delay Tplh	S/N 2 = 395.0ns S/N 5 = 428.0ns	S/N 2 = 444.0ns S/N 5 = 482.0ns	fifty 4-input AND gates in series. Low-to-high measurement.
standard buffer output voltage high Voh	S/N 2 = 4.81v S/N 5 = 4.79v	S/N 2 = 4.80v S/N 5 = 4.79v	Ioh = 3.2ma
standard buffer output voltage low Vol	S/N 2 = .075v S/N 5 = .082v	S/N 2 = .080v S/N 5 = .085v	Iol = 4.0ma
standard buffer output low short circuit Ilos	S/N 2 = 34.7ma S/N 5 = 32.6ma	S/N 2 = 33.15ma S/N 5 = 31.4ma	output buffer in low state while tied to +5v
standard buffer output high short circuit Ihos	S/N 2 = 26.8ma S/N 5 = 23.9ma	S/N 2 = 24.65ma S/N 5 = 22.20ma	output buffer in high state while tied to ground
standard input logic 0 threshold Vil	S/N 2 = 1.36v S/N 5 = 1.37	S/N 2 = 1.72v S/N 5 = 1.74v	
standard input logic 1 threshold Vih	S/N 2 = 1.38v S/N 5 = 1.39v	S/N 2 = 1.72v S/N 5 = 1.74v	
D-type flip-flop propagation delay Tdq	S/N 2 = 20.20ns S/N 5 = 22.30ns	S/N 2 = 23.15ns S/N 5 = 25.10ns	propagation delay from the D input to the Q output
frequency test Fmax	S/N 2 = 16.4Mhz S/N 5 = 14.9Mhz	S/N 2 = 14.3Mhz S/N 5 = 13.0Mhz	maximum frequency that the 12 bit binary counter will operate
dynamic Idd current Idd(dyn)	S/N 2 = 17.26ma S/N 5 = 15.45ma	S/N 2 = 29.63Mhz S/N 5 = 26.4Mhz	frequency at 5Mhz

Table 8 - Test Data for S/N 2 and 5 Post-Anneal - 70K Rad

As shown in the table 8, the other characteristics of the Actel 1280 devices showed little changes with radiation. Table 8 is data for only S/N 2 and 5 but the other parts tested exhibited similar results.

9.0 Summary

The radiation testing stopped after the 20K rad test were complete. Based on the high Idd currents seen during the exposure and annealing periods the Actel 1280 devices seem to be sensitive to the effects of radiation at levels as low as 20K rad. This test data does not conclude that the devices are not acceptable for use in a radiation environment but additional testing must be performed to assure that the high Idd currents will not significantly degrade the reliability of the devices. Additional testing at levels of 10K rad and lower will be performed by Hughes at a later date (current schedule for testing is unknown).

Appendix A

Actel 1280 FPGA
Total Dose Radiation Test Procedure
Hughes Aircraft Company
Date: 11-14-91 Rev A

I. TEST A

Objective:
- To measure electrical parameters V_{OH}, V_{OL}, I_{OS}, and leakage current of tri-state output buffers.
- To measure timing parameters Tr, Tf, T_{PHL}, T_{PLH}, T_{PHZ}, T_{PZH}, T_{PLZ}, T_{PZL}.

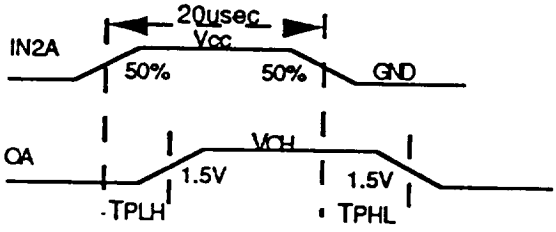
Circuit:
- Refer to Figure 1.
- A total of four Test Circuit - Tri-State Buffer's would be used in a design.

Layout:
- Refer to Figure 2.
- One test circuit would be used on each side of an Actel part.

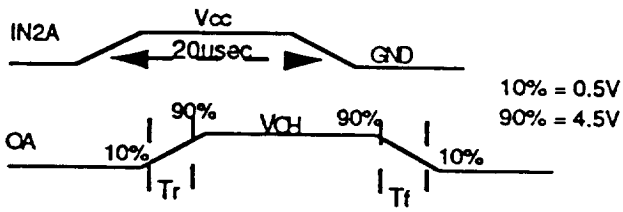
Simulation Results: NONE

Test Procedure:
- Measure electrical and timing parameters of all four test circuits.
- Measure VOH at IOH = -3.2 ma and IOH = -20 *ua*
  VOL at IOL = 4 ma and IOL = 20 *ua*.
  (TEST ONLY ONE OUTPUT AT A TIME)
- Measure output short circuit current Ios for :
  VOH shorts to GND for maximum of 20 msec.
  VOL shorts to VCC for maximum of 20 msec.
  (TEST ONLY ONE OUTPUT AT A TIME)
- Disable tri-state output buffers and measure output leakage current.
- Measure timing parameters according to the following figures:

IN1A = VCC

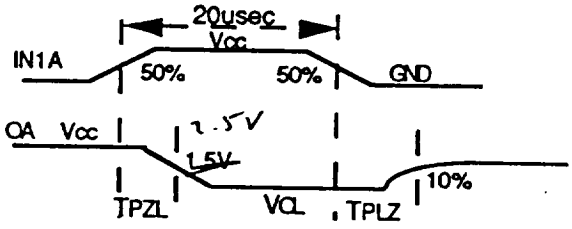


IN1A = VCC

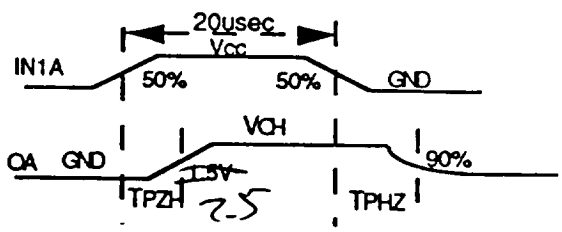


* Also measure Tr and Tf between 1V and 4 V

IN2A = GND

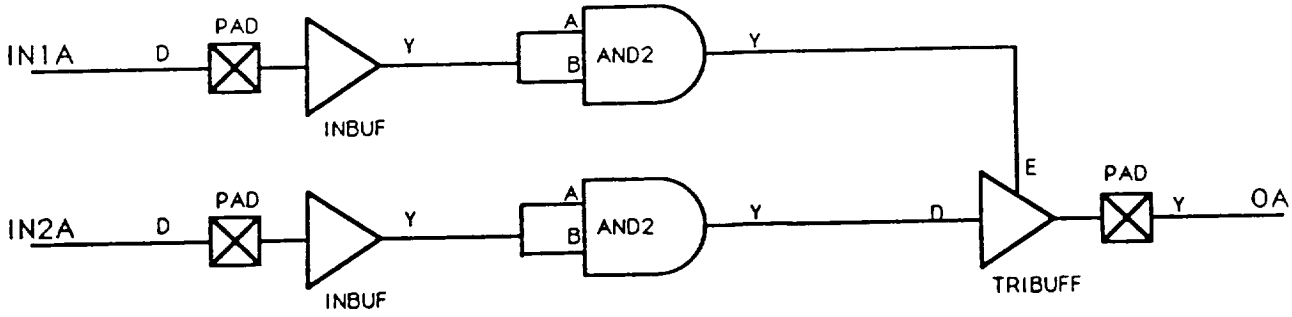


IN2A = Vcc



- Set an output to a logic low state with a voltage load of 0 V. The voltage load would be swept to 5 V in 0.5 V steps.
  Measure output current I as a function of output voltage V.

- Set an output to a logic high state with a voltage load of 5 V. The voltage load would be swept to 0 V in 0.5 V steps.
  Measure output current I as a function of output voltage V.



Test Circuit A - Schematic Diagram

II. TEST B

Objective:
- To measure propagation delay for 4 different types of combinational logic.
- To measure V_{OH},V_{OL}, and I_{OS} of output buffers.
- To measure V_{IH},, V_{IL}, and input leakage current.

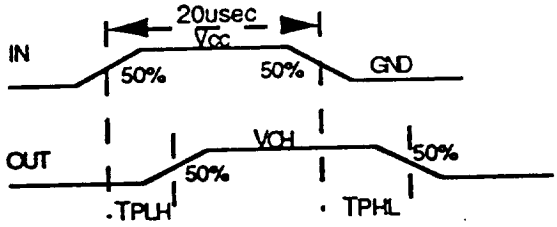
Circuit:
- Refer to Figure 3.
- Type 1 - 50 3-inputs AND gates.
- Type 2 - 50 4-inputs AND gates.
- Type 3 - 50 3-inputs OR gates.
- Type 4 - 50 4-inputs OR gates.

Layout:
- Refer to Figure 4.

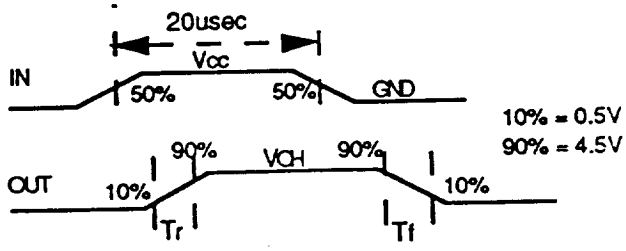
Simulation Results: Refer to Figure 5.

Test Procedure:

- Measure propagation delay from input to output of all four test circuits according to the following figure:



- Measure T_r and T_f according to the following figure:

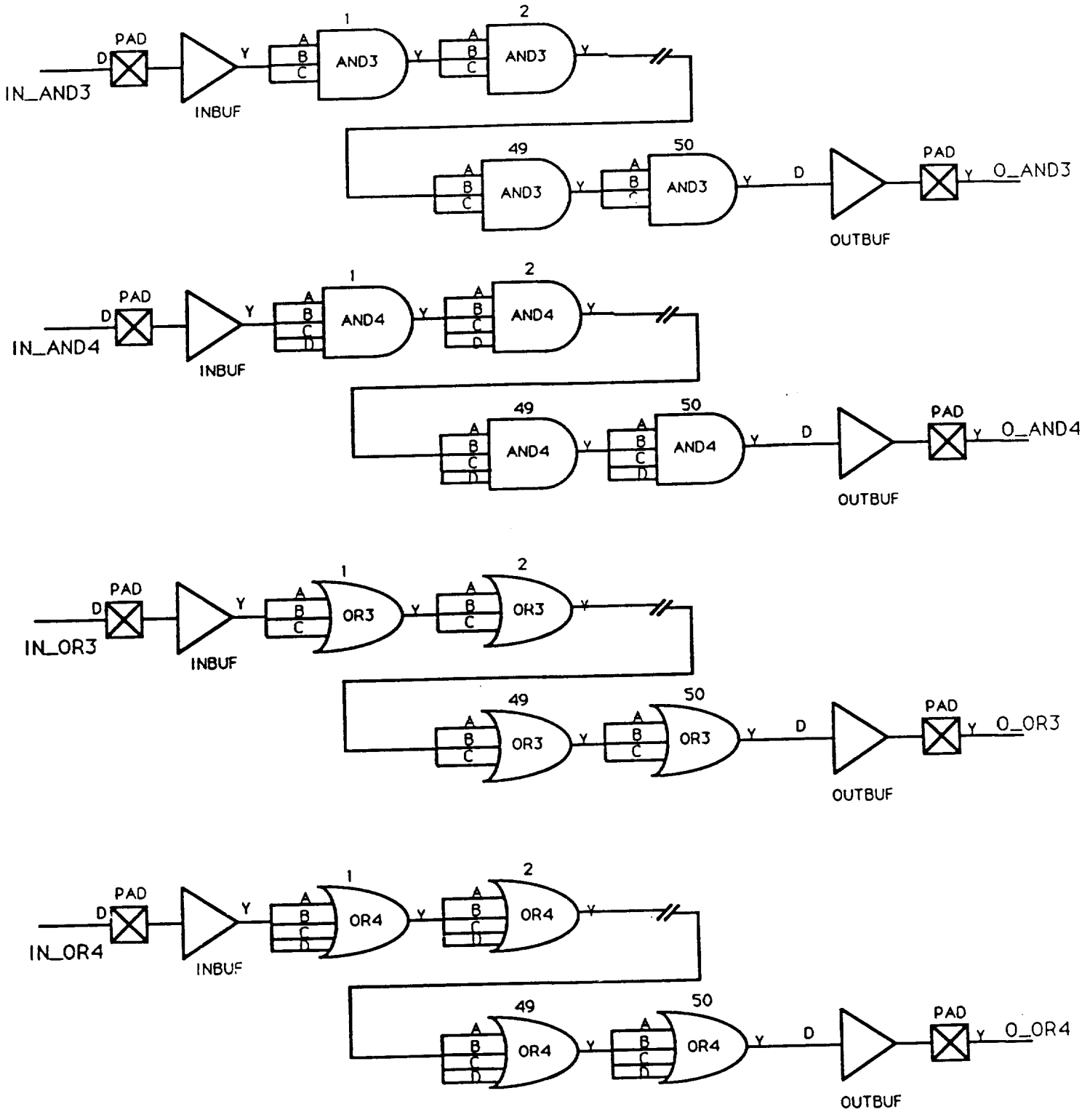


* Also measure Tr and Tf between 1V and 4 V

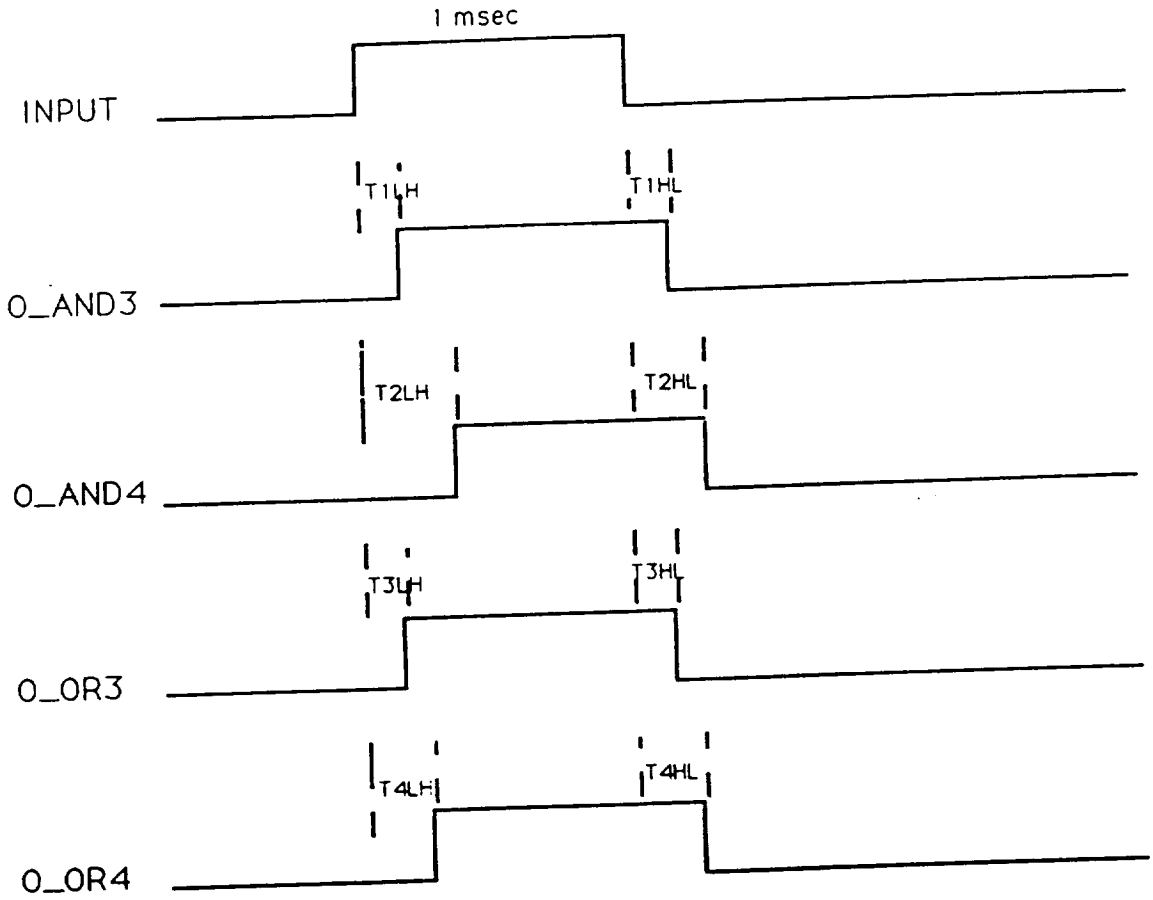
- Measure VOH at I_{OH} = -3.2 mA and I_{OH} = -20 *u*A.
  VOL at I_{OL} = 4 mA and I_{OL} = 20 *u*A.
  (TEST ONLY ONE OUTPUT AT A TIME)
- Measure output short circuit current I_{OS} for V_{OH} shorts to GND and V_{OL} shorts to Vcc for maximum of 20 msec.
  (TEST ONLY ONE OUTPUT AT A TIME)
- Measure input voltage level V_{IH} and V_{IL}.
- Measure input leakage current I_L at V_{IN} = Vcc or GND.

- Set an output to a logic low state with a voltage load of 0 V. The voltage load would be swept to 5 V in 0.5 V steps.
  Measure output current I as a function of output voltage V.

- Set an output to a logic high state with a voltage load of 5 V. The voltage load would be swept to 0 V in 0.5 V steps.
  Measure output current I as a function of output voltage V.



Test Circuit B - Schematic Diagram



AND3	T1LH =	456.1 ns	T1HL =	422.4 ns
AND4	T2LH =	863.9 ns	T2HL =	493.7 ns
OR3	T3LH =	416.1 ns	T3HL =	453.5 ns
OR4	T4LH =	497.0 ns	T4HL =	473.3 ns

Test Circuit B - Simulation Timing Diagram

III. TEST C

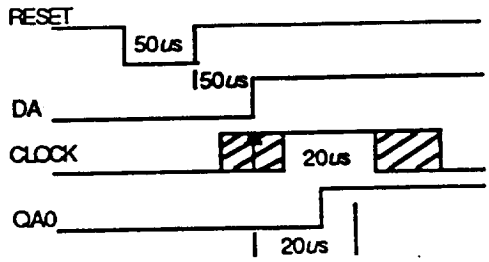
Objective:
- To measure setup and hold time, propagation delay, and minimum clock pulse width.
- To determine the clock skew.

Circuit:
- Refer to Figure 6.
- Four sets of flip-flops (A0,A1), (B0,B1), (C0,C1), and (D0,D1) would be used in the design.

Layout:
- Refer to Figure 7.
- All flip flops are manually placed. FF1 is placed closest to the clock buffer and FF2 is placed farthest from the clock buffer. Flip flops (A0,A1) and (D0,D1) are placed on different row of logic module. Flip flops (B0,B1) and (C0,C1) are placed on the same row of logic module.

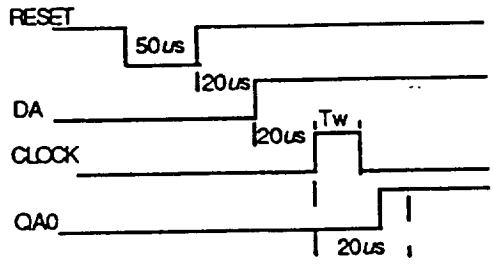
Simulation Results: Refer to Figure 8.

Test Procedure:
- Measure the setup and hold time by dithering the clock input and monitor for output QA0 according to the following figure:



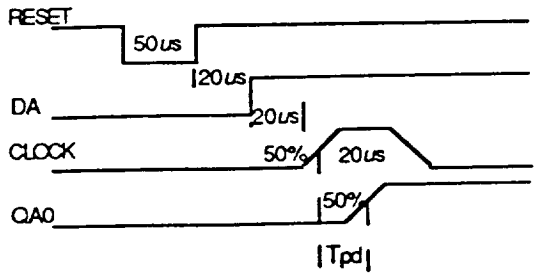
(sample QA0 20 usec after the rising edge of the clock)

- Measure the minimum clock pulse width (Tw) that triggers flip flop output QA0 to change from low to high. See the following timing diagram:

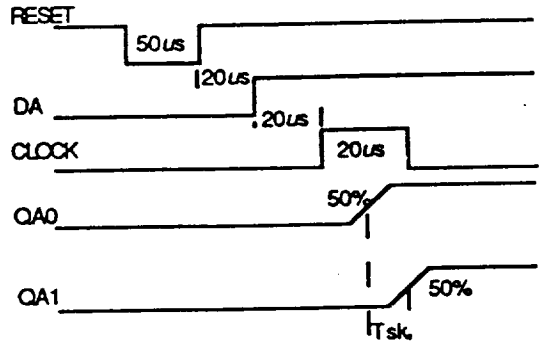


(sample QA0 20 usec after the rising edge of the clock)

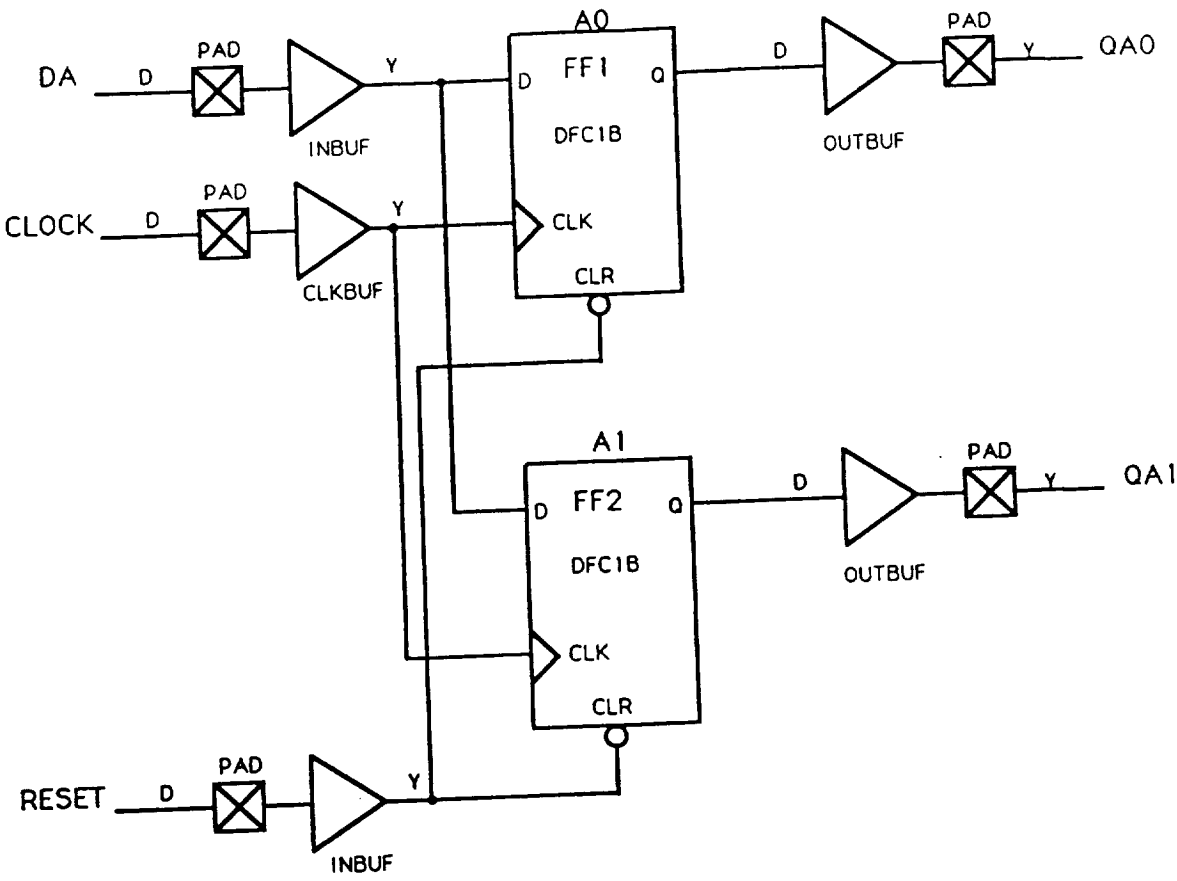
- Measure flip flop propagation delay (Tpd) according to the following figure:



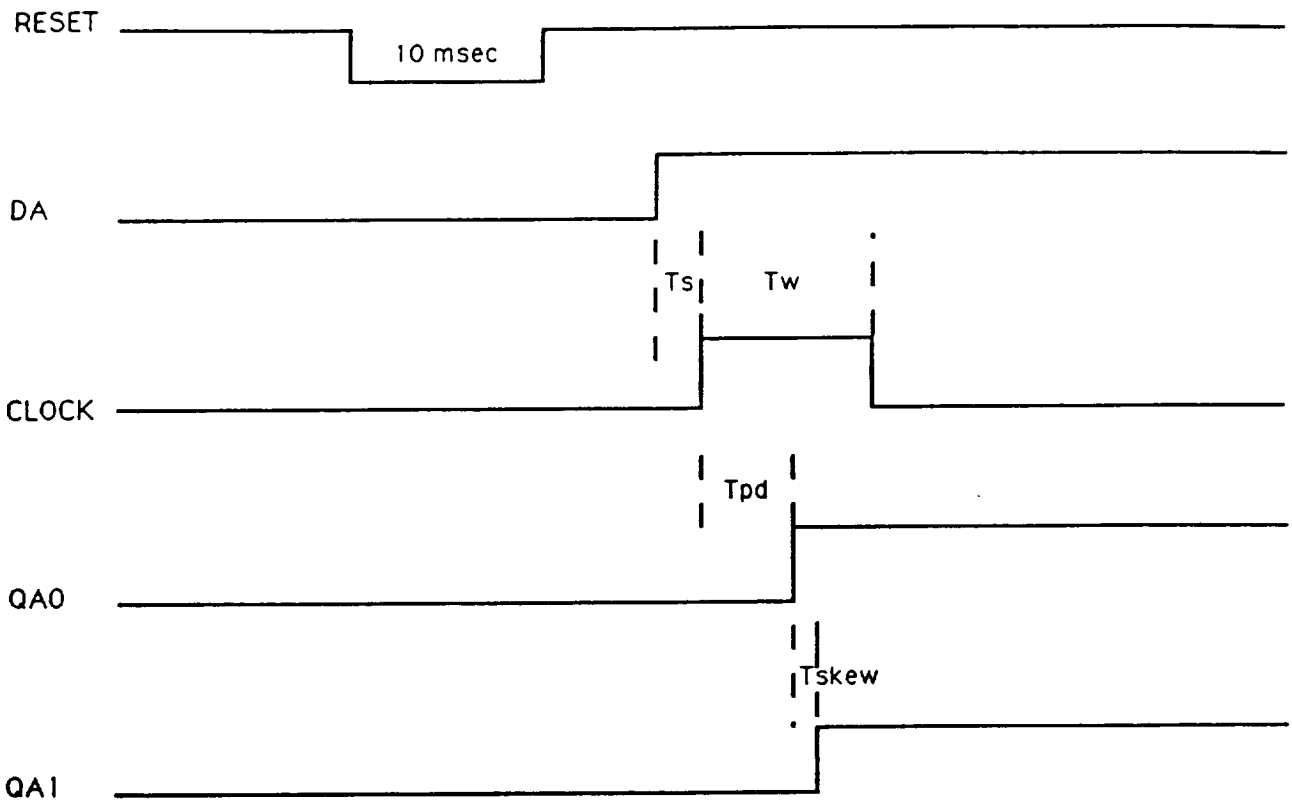
- Measure the clock skew (Tsk) according to the following figure:



- Repeat the same measurements for the other three sets (B0,B1), (C0,C1), and (D0,D1).



Test Circuit C - Schematic Diagram



Flip Flops (A0,A1):
Tsetup = 14.5 ns
Thold = 0 ns
Tpd = 23.1 ns
Tskew = 0.3 ns
Tw = 8.6 ns

Flip Flops (B0,B1):
Tsetup = 12.5 ns
Thold = 0 ns
Tpd = 24.1 ns
Tskew = -0.3 ns
Tw = 8.6 ns

Flip Flops (C0,C1):
Tsetup = 13.0 ns
Thold = 0 ns
Tpd = 23.8 ns
Tskew = -0.2 ns
Tw = 8.6 ns

Flip Flops (D0,D1):
Tsetup = 18.0 ns
Thold = 0 ns
Tpd = 23.5 ns
Tskew = 0.7 ns
Tw = 8.6 ns

Test Circuit C - Simulation Timing Diagram

IV. TEST D

Objective: - To characterize performance and Vdd minimum.

Circuit: - Refer to Figure 9.

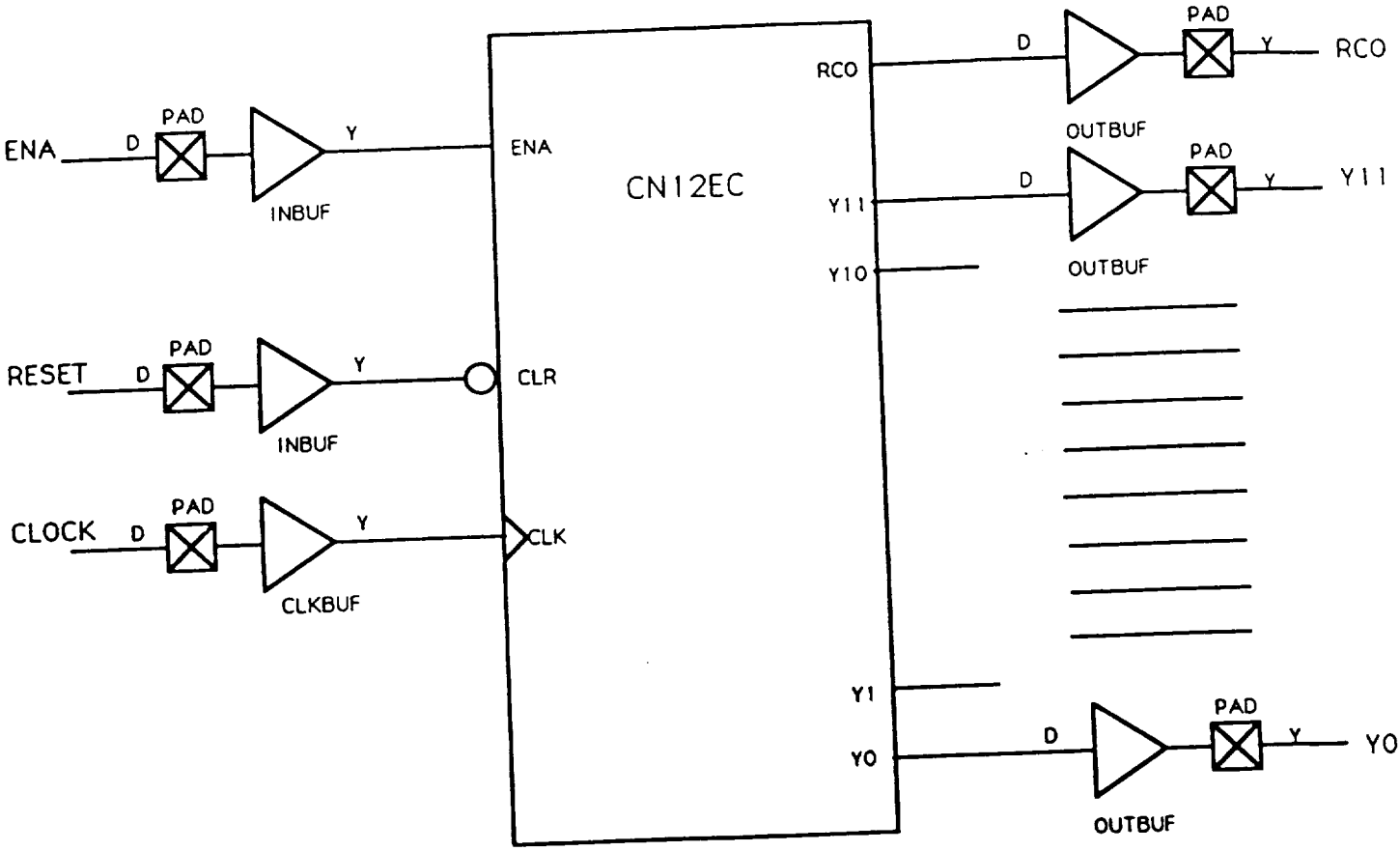
Layout: - Refer to Figure 10.

Simulation Test Results: NONE

Test Procedure:

- Characterize performance.
  a. Set ENA to logic 1.
  b. Clock Rate = 10 Mhz (TBR)
  c. Increase clock rate by 0.2 Mhz (TBR)
  d. Enable RESET for 10 msec.
  e. Verify counter outputs change from 000 through FFF and back to 000.
  f. Repeat steps c through e until the counter outputs are invalid.
  g. Record the last clock rate (ie. the clock rate at which the counter starts failing).

- Characterize Vdd minimum.
  - Set ENA to logic 1.
  - Enable Reset for 10 msec (TBR).
  - Clock Rate = 1 MHz.
  - Reduce Vdd until counter outputs are invalid.



Test Circuit D - Block Diagram

V. TEST E

Objective: - To measure Icc current.

Circuit: - Refer to Test Circuit A, B, C, and D.

Layout: - Refer to Test Circuit A, B, C, and D.

Simulation Test Results: NONE

Test Procedure:

- Measure standby current Icc.
  - All inputs = GND except RESET.
  - Set RESET to logic 0 for 10 msec.
  - Set RESET to logic 1. Measure Icc current.

- Measure operating current Icc.
  - Set RESET to logic 0 for 10 msec. Set RESET to logic 1.
  - All inputs = Vcc except inputs DA, DB, DC, DD, and CLOCK.
  - CLOCK input is 5 MHz.
  - Inputs DA, DB, DC, and DD (pin number 63,76,59, and 57) are toggled at 2.5 MHz on the falling edge of 5 MHz clock.

SECTION 4.0
Actel 1020A (1.2 μm)

SECTION 4.1
Radiation Data Total Dose

PRODUCT: ACTEL CMOS FPGA
MANUFACTURING BY: MATSUSHITA ELECTRONICS CORP.
DEVICE: A1020A 1.2 micron 2000 gates
EVALUATED BY: TRW Electronics System Group
Ref.TRW H936.12.TCL

RADIATION TOTAL DOSE

3 units were evaluated at 30, 50, 100, and 200 krads(Si) total dose at a dose rate of 79 rads(Si)/sec per Mil-Std-883 method 1019.The devices were irradiated in a single exposure sequence. Two units were used as control. Bias on pins during exposure were selectively set to high, low, or open. All units were 84 pin, J lead, plastic package, commercial grade supplied by Actel.

PARAMETRIC AND FUNCTIONAL RESULTS

Conditions: There was no delay between radiation and test, nor was there bias maintained between radiation and test.

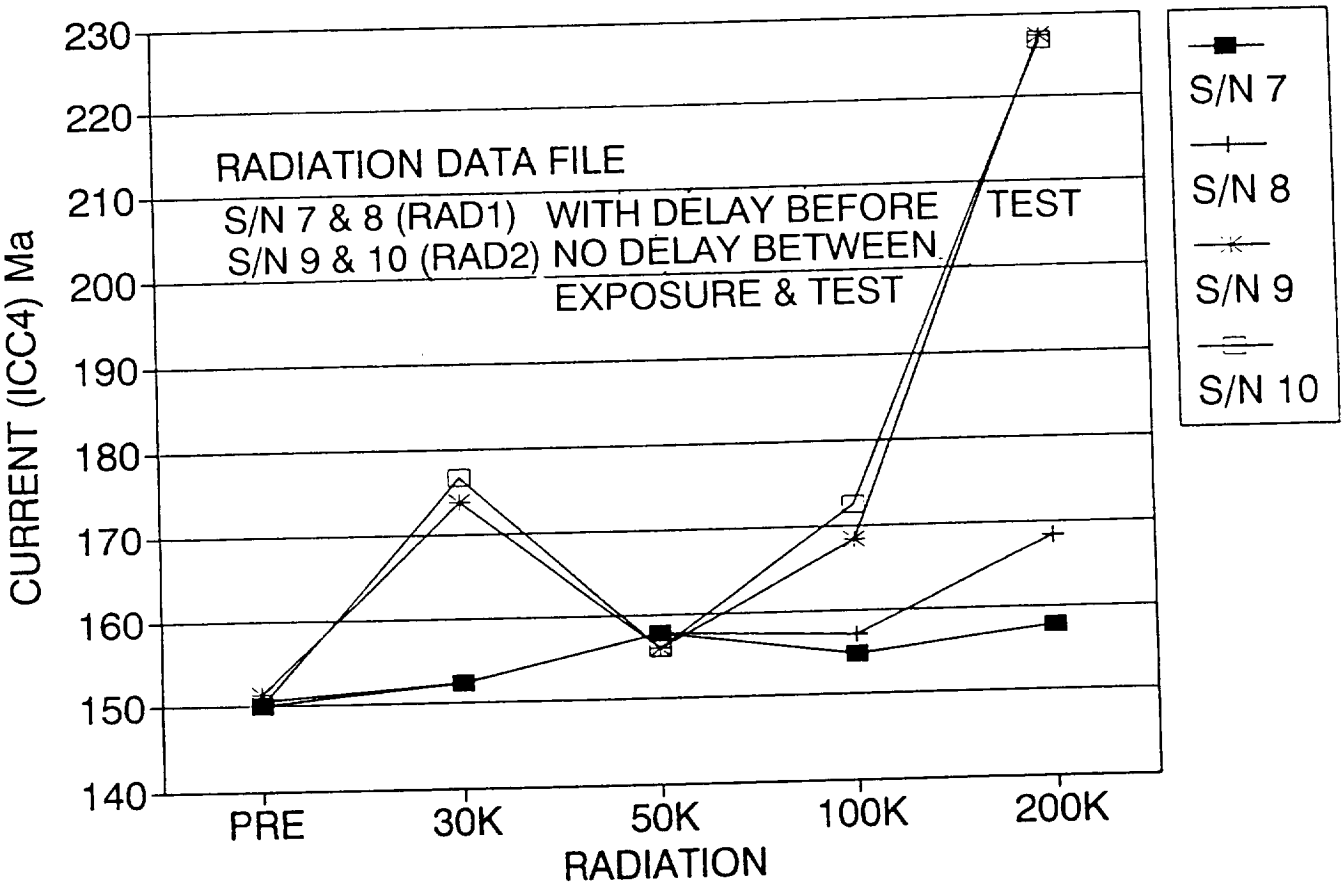
Unit # 12	0K(Pre)	30K	50K	100K	200K	Anneal (24hrs)
VIH	Pass	Pass	Pass	Pass	Pass	
VIL	Pass	Pass	Pass	Pass	Pass	
IIH	Pass	Pass	Pass	Pass	Pass	
IIL	Pass	Pass	Pass	Pass	Pass	
IOH	Pass	Pass	Pass	Pass	Pass	
IOL	Pass	Pass	Pass	Pass	Pass	
tPHL	Pass	Pass	Pass	Pass	Pass	
tPLH	Pass	Pass	Pass	Pass	Pass	
VOH	Pass	Pass	Pass	Pass	Pass	
VOL	Pass	Pass	Pass	Pass	Pass	
ICC(ac)	150.6	211.3	199.4	222.6	242.9	190
ICC(dc)	3.5	63.7	52.4	72.6	86.3	
FUNC	Pass	Pass	Pass	Pass	Pass	

Unit #13	0K(Pre)	30K	50K	100K	200K	Anneal (24hrs)
VIH	Pass	Pass	Pass	Pass		
VIL	Pass	Pass	Pass	Pass		
IIH	Pass	Pass	Pass	Pass		
IIL	Pass	Pass	Pass	Pass		
IOH	Pass	Pass	Pass	Pass		
IOL	Pass	Pass	Pass	Pass	Fail	
tPHL	Pass	Pass	Pass	Pass		
tPLH	Pass	Pass	Pass	Pass		
VOH	Pass	Pass	Pass	Pass		
VOL	Pass	Pass	Pass	Pass		
ICC(ac)	151.2	219.7	204.8	225.6	245	206
ICC(dc)	3.5	70.2	55.9	75.0		
FUNC	Pass	Pass	Pass	Pass	Fail	

Unit #15	0K(Pre)	30K	50K	100K	200K	Anneal (24hrs)
VIH	Pass	Pass	Pass	Pass	Pass	
VIL	Pass	Pass	Pass	Pass	Pass	
IIH	Pass	Pass	Pass	Pass	Pass	
IIL	Pass	Pass	Pass	Pass	Pass	
IOH	Pass	Pass	Pass	Pass	Pass	
IOL	Pass	Pass	Pass	Pass	Pass	
tPHL	Pass	Pass	Pass	Pass	Pass	
tPLH	Pass	Pass	Pass	Pass	Pass	
VOH	Pass	Pass	Pass	Pass	Pass	
VOL	Pass	Pass	Pass	Pass	Pass	
ICC(ac)	152.4	217.3	204.8	225.6	248.8	210
ICC(dc)	3.5	66.7	55.4	73.8	95.8	
FUNC	Pass	Pass	Pass	Pass	Pass	

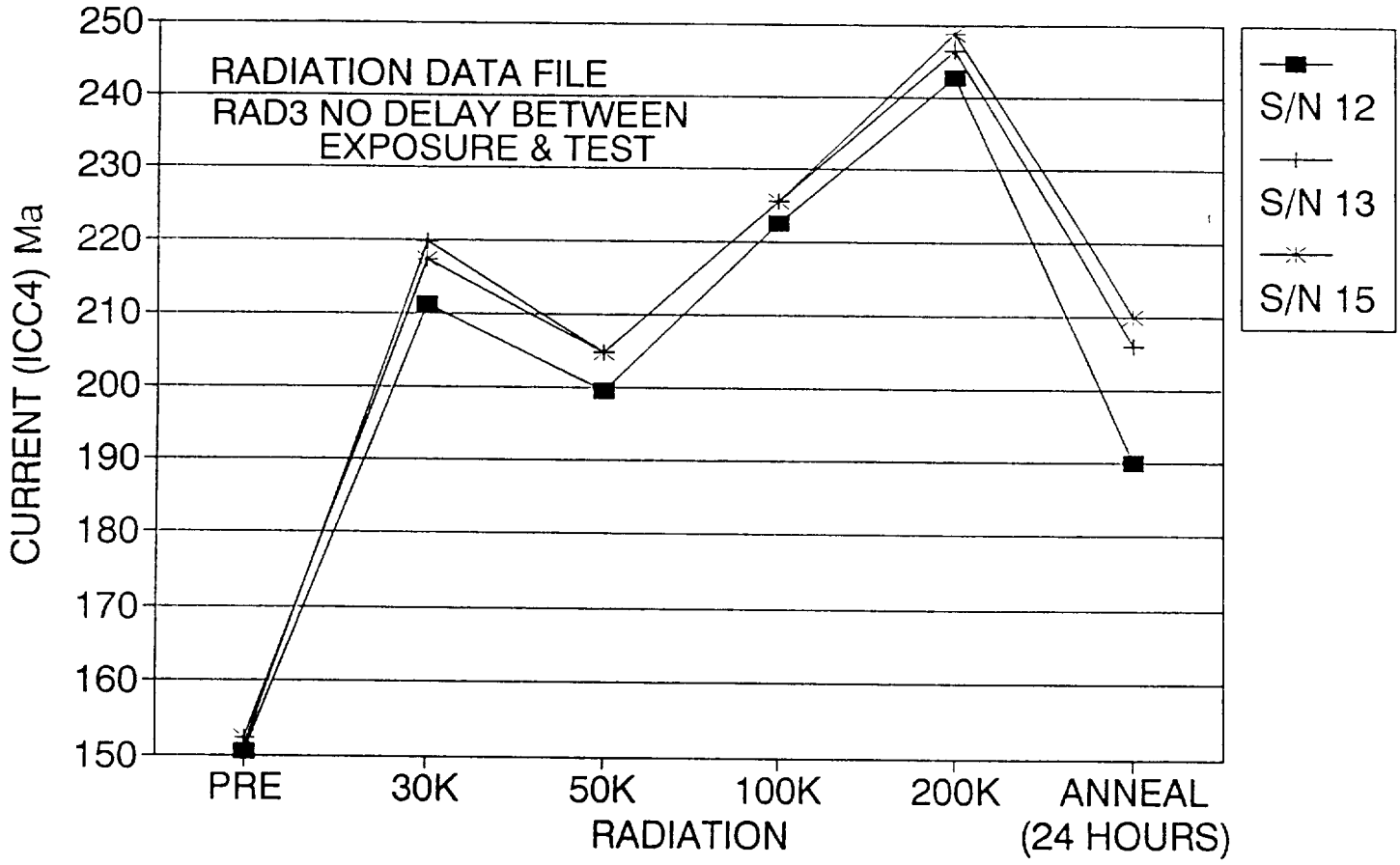
TOTAL DOSE OF A1020A

ACTEL FPGA (1.2 MICRON, MEC DIE)



TOTAL DOSE OF A1020A

ACTEL FPGA (1.2 MICRON, MEC DIE)



SECTION 4.2
Current Density/Step Coverage

TRW SUMMARY REPORT

PRODUCT: ACTEL CMOS FPGA
MANUFACTURING BY: MATSUSHITA ELECTRONICS CORP.
DEVICE: A1020A 1.2 micron 2000 gates
EVALUATED BY: TRW Electronics System Group
Ref. TRW R212.4-027/92 and R212.4-028/92

EVALUATIONS:

METAL STEP COVERAGE

Metal step coverage for contact and via is less than 30% per MIL-STD-883 Method 2018. Method of analysis SEM and metallographic sectioning. Worst case side of via or contact was used for measurement.

METAL CURRENT DENSITY

Current density was calculated at less than 2.0×10^{5} A/cm^{2} allowed by MIL-M-38510 (This assumes 1ma per contact worst case as dictated by ACTEL design rule)

Specific current density calculated is 1.1 ma/um^{2} or 1.1×10^{5} A/cm^{2} at contacts.

No cracks or opens in metal were seen at contacts.

LIFE TEST RESULTS

44 Units completed 2000 hours of accelerated life test with no functional failures. Test conditions were Vsig =5.5Vpp, Vcc = 5.75V, and f = 1 MHZ(Vsig).

All units exhibited an IOL drift (measure is in ma) of between 12% and 18%. This occurred on the majority of units and device pins tested for IOL. Good pins on the same device showed less than 3% drift. This parametric change may be caused by problems associated with the CMOS N-ch transistors and should be further investigatied. The maximum change occured after 2000 hours of life test with the greatest increase occuring in the first 500 hours. VOL also showed a similiar drift which tracked the IOL drift. All other parameters demonstrated less than 5% change throughout the life test.

ACCELERATION FACTOR AND LIFE PREDICTION

Acceleration factors were calculated using a junction temperature of 187°C and an estimated activation energy of 0.6ev. The field application temperature ranged from 30°C to 130°C. The acceleration factors ranged from 252E+03 to 8.48E+00. Life predictions for this range and the above junction temperature were calculated at 575 years to 1.90 years.

HI-REL
LABORATORIES

911 SOUTH MOUNTAIN AVE. • MONROVIA • CALIFORNIA 91016 • (818) 357-6083 • FAX (818) 357-6913

TRW Systems
One Space Park
Redondo Beach, Ca. 90278

Report Number MR-101033
Report Date: October 18, 1991
P.O. Number: SR437026
Date Received: October 4, 1991

REPORT OF LABORATORY ANALYSIS

DESCRIPTION OF SAMPLES: One (1) A1020A, ACTEL FPGA, S/N 11

METHOD OF ANALYSIS: Depot, SEM, Metallographic Sectioning, and SEM.

FINDINGS: One (1) A1020A, Actel FPGA, serial number 11, was submitted for evaluation of the metallization step coverage by means of metallographic sectioning. The device was chemically decapsulated to expose the die surface so that metallization stripe width measurements could be obtained. The device was then encapsulated in epoxy and prepared using precision metallographic techniques. The following results were obtained:

Location	* Minimum Metal Thickness	*% Original Metal Remaining
Via 1	0.18 Microns	19%
Via 2	0.19 Microns	20%
Contact 1	0.09 Microns	11%
Contact 2	0.10 Microns	13%
Contact 3	0.04 Microns	4.5%

* Worst case side of via or contact used for measurement.

Silicon nodules were noted in the metallization but were not taken into consideration in any measurements.

I certify that this report truly represents the findings of work performed by me or under my supervision.

Trevor A. Devaney

Reviewed and Approved By:

John R. Devaney

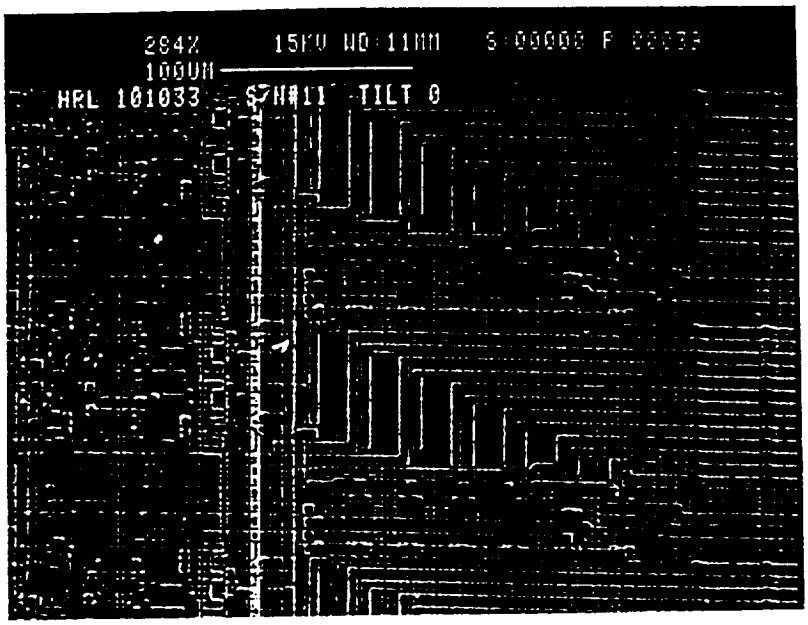


Figure 1: General SEM view of typical metallization with the glassivation on. Mag. (284X)

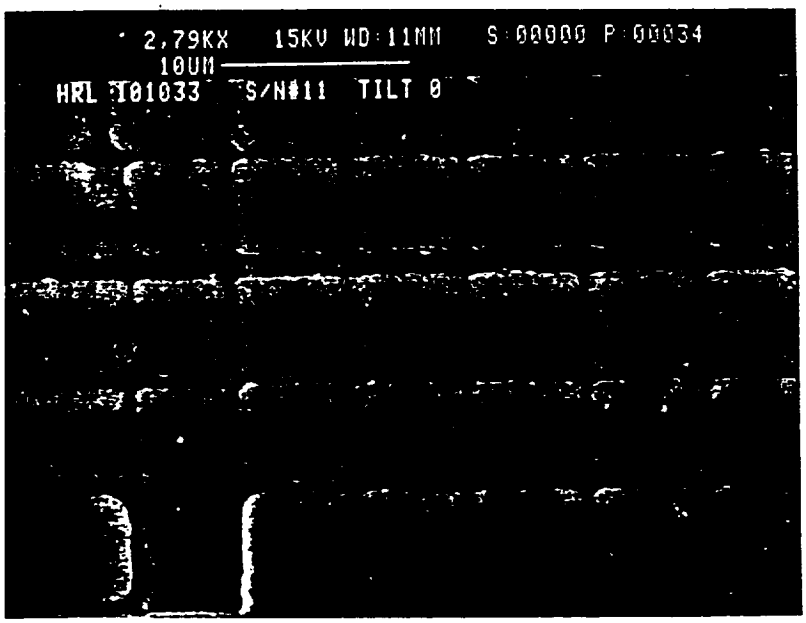


Figure 2: Detailed view of typical metal stripes. Width is ~ 4.5 Microns. Mag. (2.79Kx)

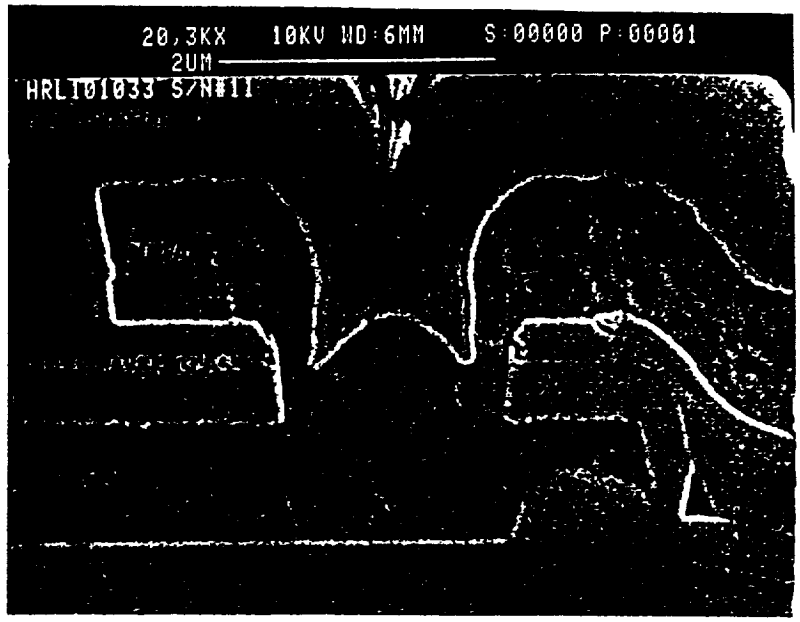


Figure 3: Detailed cross-sectional view of via 1. Mag. (20.3Kx)

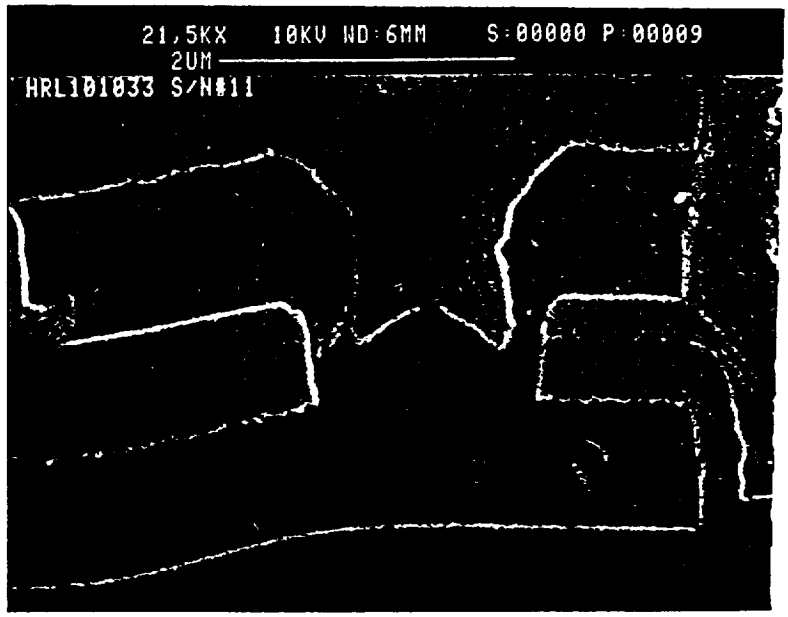


Figure 4: Detailed cross-sectional view of via 2. Mag. (21.5Kx)

Figure 5: Detailed cross-sectional view of contact 1. mag. (29.4Kx)

Figure 6: Detailed cross-sectional view of contact 2. Note large silicon nodule at step. Mag. (29.4Kx)

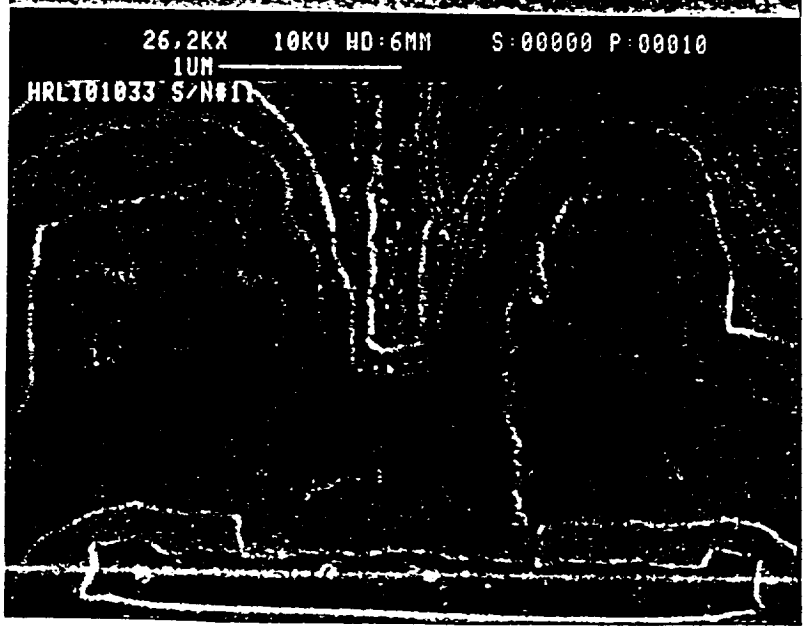


Figure 7: Detailed cross-sectional view of contact 3. Note severe thinning at step. Mag. (26.2Kx)

S. Chiang and W.V.D. Abeelen
Actel Corp.

Electromigration Summary of Actel 1020A 1.2um process from MEC Foundry

Expected lifetimes of vias, contacts and metal lines.

Lifetime of vias and contacts of Actel's 1.2um 1020A product is simulated to be greater than 100 years at 100C junction temperature. As actually performed by Electromigration Burn-in test of the product, the lifetime exceeds more than 20 years, with no EM related failures found thus far.

We expect longer lifetimes for the vias and contacts of the 2.0 um 1020 product. Via and contact size on silicon is 2.0 um for the 2.0 um process, while it is 1.5 um for the 1.2 um process.

Metal 1 and Metal 2 lines exceed over 40 years at 100C as performed by EM burn-in test.

Actual current through single contacts and vias

Based on simulations of a 33 MHz clock frequency design, we found that single contacts/vias passed no more than 100uA in DC current. This is significantly lower than the current allowed to pass through a contact or via. All the single contacts singled out in the JPL report(Ref. 1) passed no more than 65uA at 33MHz and 100C junction temperature.

Another issue mentioned in the above memo suggested that 4mA output buffer current went through either single or multiple contacts. The 4mA was distributed over 36 contacts(equal to 110uA per contact). The worst case single contact in the output buffer was a gate-poly contact, carrying 170 uA of AC current.

Effect of poor step coverage on the electromigration calculations.

The maximum current density allowed in Actel's electromigration rules, has already taken into consideration that metal lines over topographic structures will reduce its EM capability. The rules also reflect the fact that it is applicable over the whole process spectrum. In addition, runs to be selected for space application have better than average step coverage and line width reduction, based on metal resistance evaluation from the process monitor test chip.

Observation of nodules inside the contact, via or metal lines.

The metal system has 1% silicon, 0.5% copper in aluminum. Nodules are expected to occur. The electromigration rule has taken into consideration the fact that there will be nodules and that they will reduce the step coverage. The nodule size is small and it does not break the interconnect.

Future improvement

In the new 1.0 um process, barrier metals are used for both Metal 1 and Metal 2. The expected EM lifetime for the 1.0 um products are hereby greatly improved.

References

[1] Mike Sander, "Calculation of current density for Actel 2.0um Technology" , Jet Propulsion Laboratory, Feb. 14 1992

EM1020A5.DOC

SECTION 4.3
Life Test/Characterization

TRW SUMMARY REPORT

PRODUCT: ACTEL CMOS FPGA
MANUFACTURING BY: MATSUSHITA ELECTRONICS CORP.
DEVICE: A1020A 1.2 micron 2000 gates
EVALUATED BY: TRW Electronics System Group
Ref. TRW R212.4-027/92 and R212.4-028/92

EVALUATIONS:

METAL STEP COVERAGE

Metal step coverage for contact and via is less than 30% per MIL-STD-883 Method 2018. Method of analysis SEM and metallographic sectioning. Worst case side of via or contact was used for measurement.

METAL CURRENT DENSITY

Current density was calculated at less than 2.0×10^{5} A/cm^{2} allowed by MIL-M-38510 (This assumes 1ma per contact worst case as dictated by ACTEL design rule)

Specific current density calculated is 1.1 ma/um^{2} or 1.1×10^{5} A/cm^{2} at contacts.

No cracks or opens in metal were seen at contacts.

LIFE TEST RESULTS

44 Units completed 2000 hours of accelerated life test with no functional failures. Test conditions were Vsig =5.5Vpp, Vcc = 5.75V, and f = 1 MHZ(Vsig).

All units exhibited an IOL drift (measure is in ma) of between 12% and 18%. This occurred on the majority of units and device pins tested for IOL. Good pins on the same device showed less than 3% drift. This parametric change may be caused by problems associated with the CMOS N-ch transistors and should be further investigatied. The maximum change occured after 2000 hours of life test with the greatest increase occuring in the first 500 hours. VOL also showed a similiar drift which tracked the IOL drift. All other parameters demonstrated less than 5% change throughout the life test.

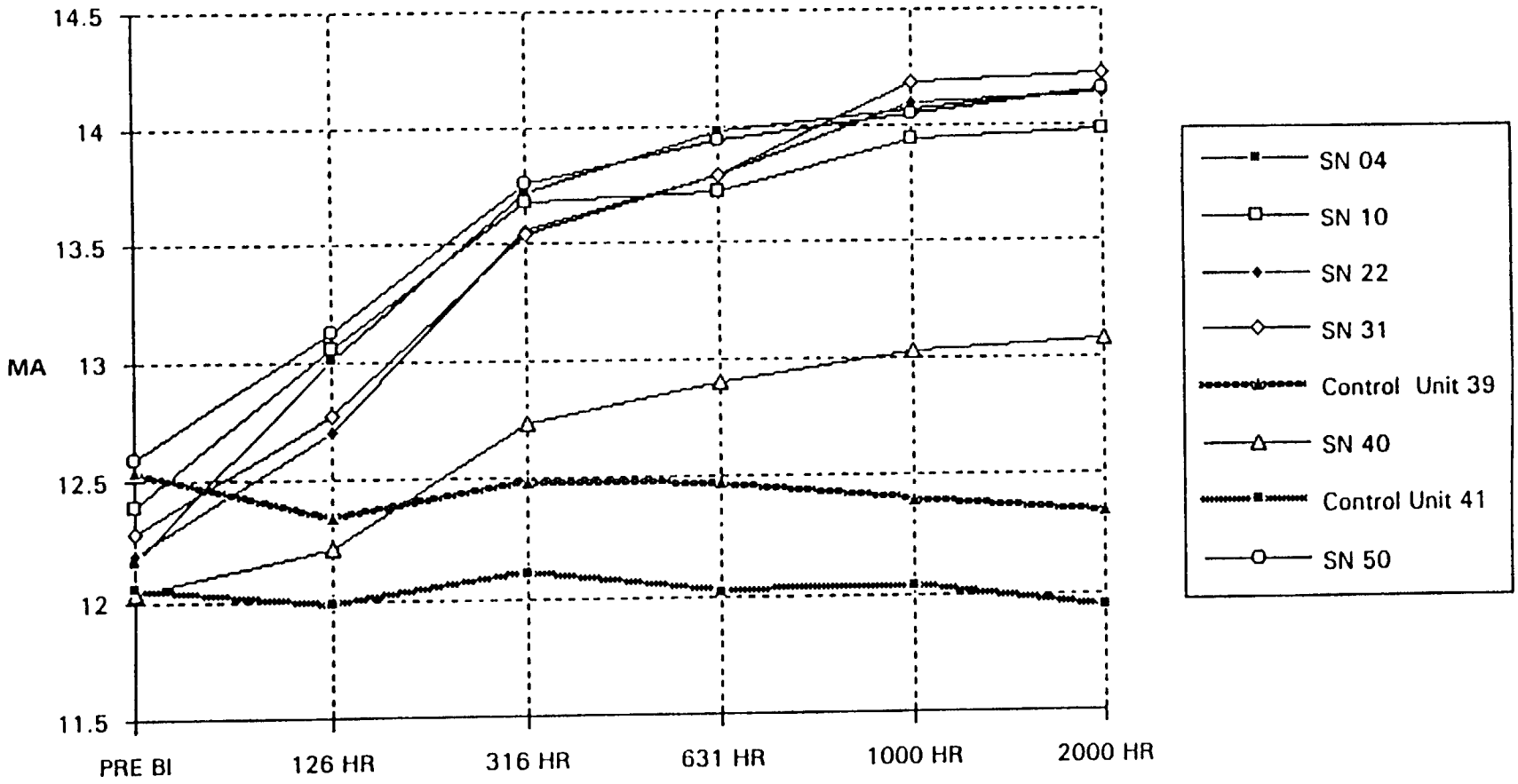
ACCELERATION FACTOR AND LIFE PREDICTION

Acceleration factors were calculated using a junction temperature of 187°C and an estimated activation energy of 0.6ev. The field application temperature ranged from 30°C to 130°C. The acceleration factors ranged from 252E+03 to 8.48E+00. Life predictions for this range and the above junction temperature were calculated at 575 years to 1.90 years.

LIFE TEST

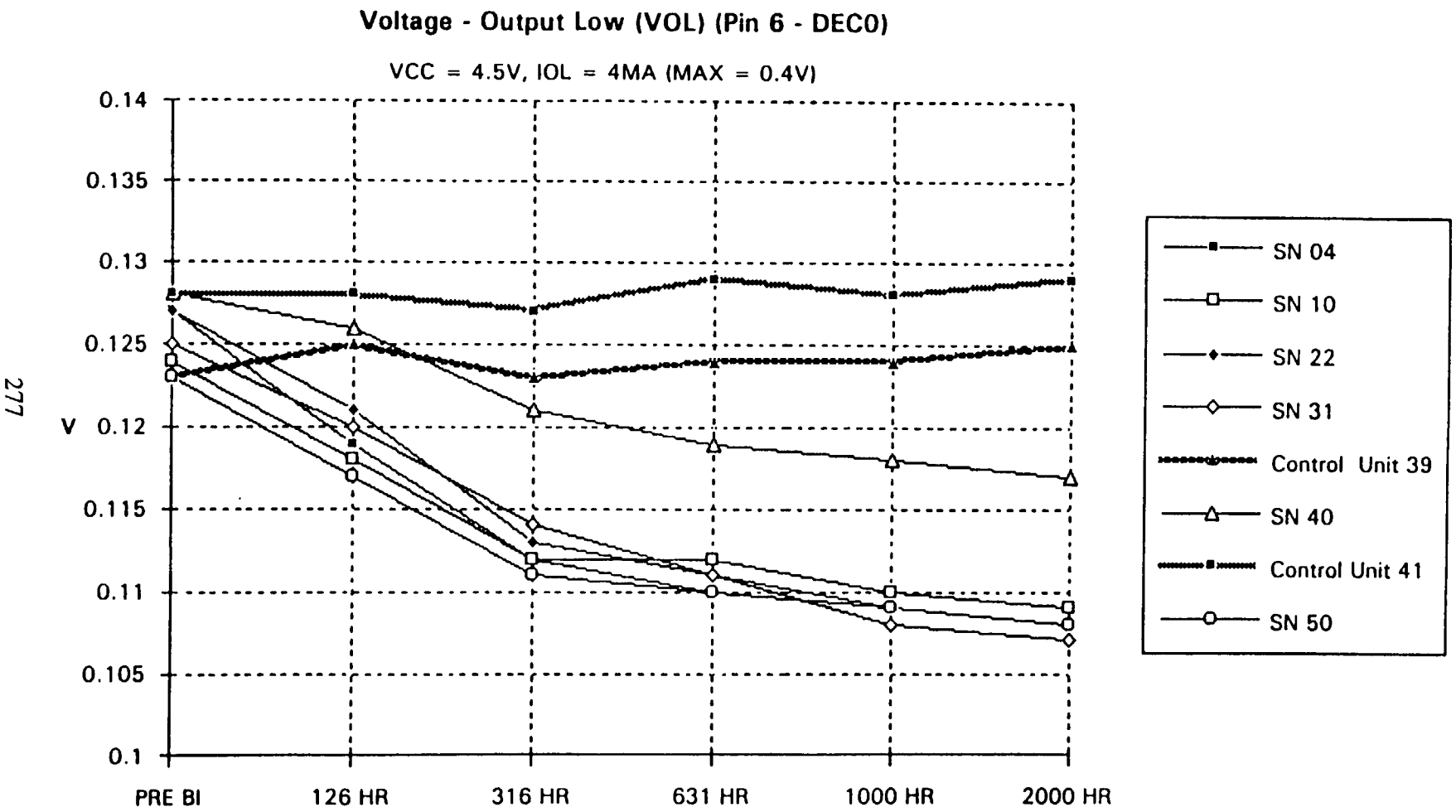
Current - Output Low (IOL) (Pin 6 - DEC0)

VCC = 4.5, VIOL = 0.4V (MIN = 4.0MA)



3/30/92

IOL.XLC



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VOL.XLC

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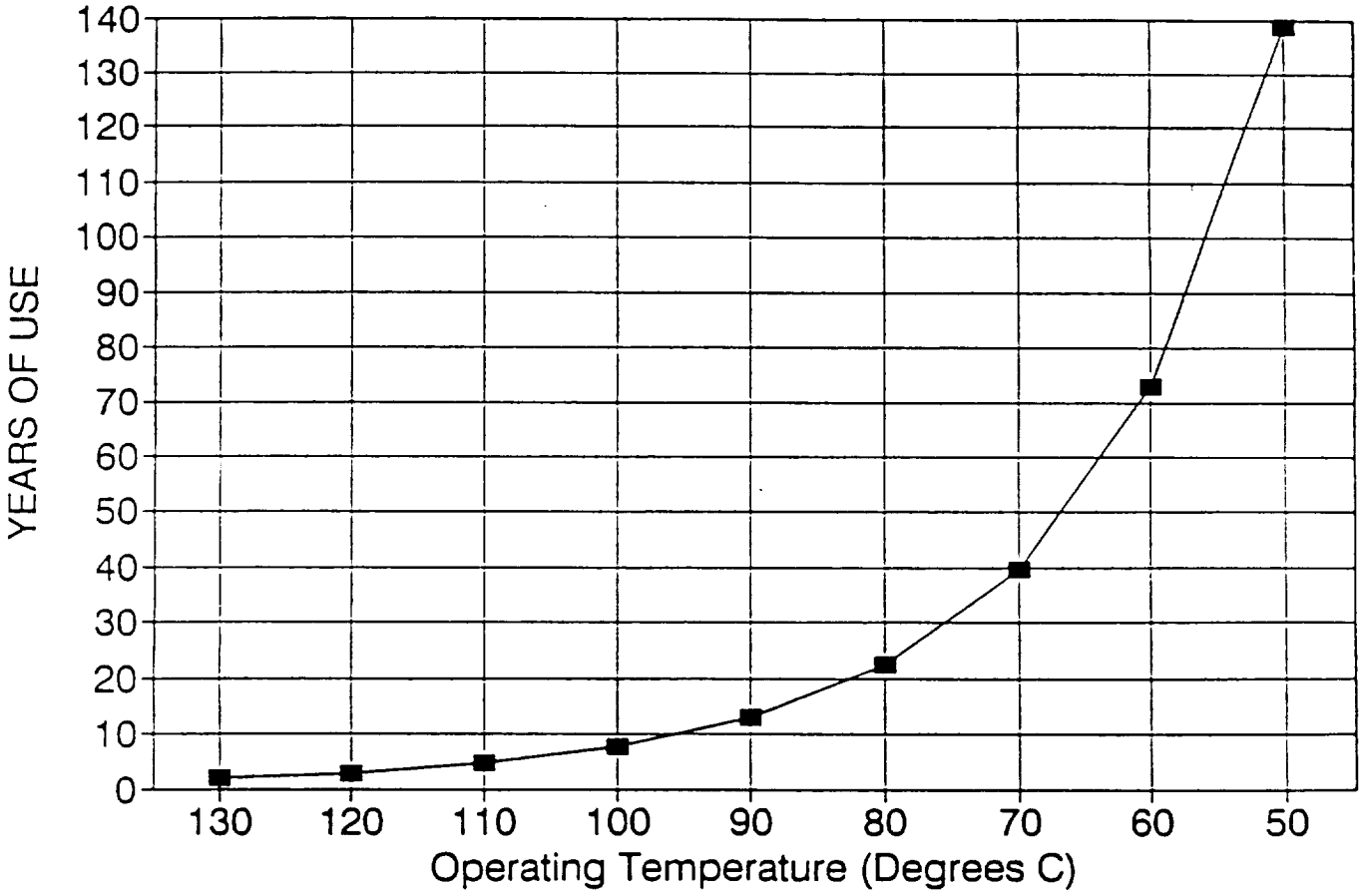
Acceleration Factor Calculations

Acceleration Factor (A.F.) = exp((activation energy/K)(1/Tdesign - 1/Ttest)
K = Boltzman's constant = 8.63E-5 eV/degree kelvin(K)
Activation Energy = 0.6eV (estimated)

Ttest = oven temp + theta ja for ceramic quad flatpack
in still air, [(40 C/W) * (I * V)] + 273 (for Kelvin conversion)

Tdesign	Ttest	A.F.	Mission Life (yrs)
45	187	8.53E+02	194.8
50	187	6.08E+02	138.9
55	187	4.38E+02	50.0
60	187	3.19E+02	72.8
65	187	2.34E+02	53.4
70	187	1.73E+02	39.6
75	187	1.30E+02	29.6
130	187	8.48E+00	1.9
120	187	1.32E+01	3.0
110	187	2.09E+01	4.8
100	187	3.40E+01	7.8
90	187	5.68E+01	13.0
80	187	9.76E+01	22.3
70	187	1.73E+02	39.6
60	187	3.19E+02	72.8
50	187	6.08E+02	138.9
40	187	1.21E+03	276.2
30	187	2.52E+03	575.0

PREDICTED YEARS OF USE
BASED ON 2000 HOUR LIFE TEST DATA



TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No. JPL Pub. 92-22	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle Field Programmable Gate Arrays: Evaluation Report for Space-Flight Application		5. Report Date September 15, 1992 6. Performing Organization Code
7. Author(s) Mike Sandor, Mike Davarpanah, Kamal Soliman, et al.		8. Performing Organization Report No.
9. Performing Organization Name and Address JET PROPULSION LABORATORY California Institute of Technology 4800 Oak Grove Drive Pasadena, California 91109		10. Work Unit No. 11. Contract or Grant No. NAS7-918
12. Sponsoring Agency Name and Address NATIONAL AERONAUTICS AND SPACE ADMINISTRATION Washington, D.C. 20546		13. Type of Report and Period Covered JPL Publication 14. Sponsoring Agency Code RE65 FY42638000617: 50% RE256 BP45157BAFA00: 50%
15. Supplementary Notes		

16. Abstract

Field Programmable Gate Arrays commonly called FPGA's are the newer generation of field programmable devices and offer more flexibility in the logic modules they incorporate and in how they are interconnected. The flexibility, the number of logic building blocks available, and the high gate densities achievable are why users find FPGA's attractive. These attributes are important in reducing product development costs and shortening the development cycle. The aerospace community is interested in incorporating this new generation of field programmable technology in space applications. To this end a consortium was formed to evaluate the quality, reliability, and radiation performance of FPGA's. This report presents the test results on FPGA parts provided by ACTEL Corporation.

17. Key Words (Selected by Author(s)) Components	18. Distribution Statement Unclassified -- Unlimited		
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 279	22. Price

JPL 0184 R 9/83